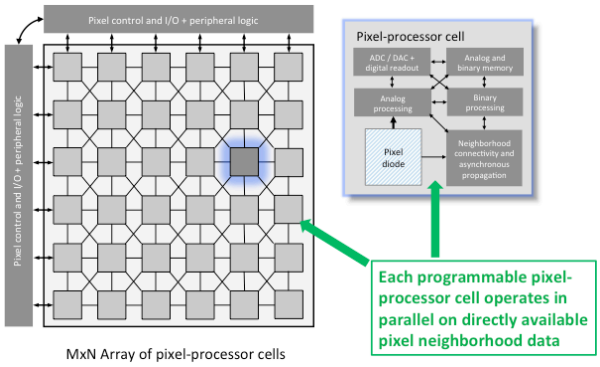
Visual Simultaneous Localization and Mapping using Focal-place Processors

Description

This project targets implementing Visual SLAM (simultaneous localization and mapping) for robotics with focal-plane (FP) processors and efficient parallel image analysis methods. FP processors are massively-parallel in-pixel processing architectures. The use of FP processing enables a radical reduction of the data applied to the mapping and decision making system, and therefore allows novel real-time, CMOS camera only, robot control algorithms.

The use of extremely efficient sensor-level parallel processing (i.e. focal-plane processing) for the extraction of both spatial and temporal feature information from visual data is studied. This includes e.g. the detection of spatial salient features, such as corner, edges and object planes, as well as temporal segmentation based e.g. on extracting foreground and background movement from optical flow or structure from motion. The fact that the FP technique provides faster frame rates than conventional cameras allows us to use different time scales to dynamically separate moving objects from the background. While conventional cameras provide too much data for energy-efficient off-chip processing, the FP solution realizes the most computationally intensive low- and mid-level processing already within the sensor chip. For detecting and describing local features in images and optical flow many widely known algorithms (e.g. SIFT, SURF, Lucas-Kanade) exist. For most of these, to achieve real-time performance, HW or GPU acceleration is currently the only option. The suitability of these algorithms (and / or the concepts they embrace) for FP will be investigated.



The graduation assignment

We expect the following of you:

1. Analysis, simulation, and coding of common algorithms used for monocular visual SLAM. To be able to choose the best algorithms suited for FP.
2. FP parallelization of the results for FP processors.

Background requirements: Video algorithms basics, embedded design basics, matlab, programming basics. Familiarity with HDL languages is a benefit, but not required.

The work will be done at the Technology Research Center (trc.utu.fi), Finland in close collaboration with the leading FP manufacturer Kovilta (www.kovilta.fi), Finland and the Electronic Systems group of the TU/. The work is part of the ALMARVI European research project (www.almarvi.eu).

More information

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