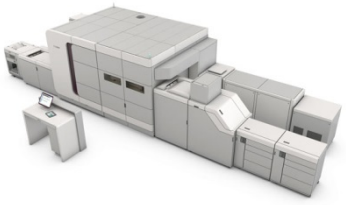
Graduation project:
Multi-core Datapath Contention Modelling

Description

The *datapath* is a central part of printers and copiers and is responsible for the image processing that is necessary to produce output of required quality. A key performance indicator of the datapath is its performance, typically expressed as throughput in processed image-data per minute. The operations in the datapath are data-intensive and are often implemented in software on multi-core embedded platforms. The programming can thus have a significant effect on the performance through its use of the data caches. Currently performance offered by platform components rapidly increases. The graduation assignment is to analyze and optimize the image processing in print datapaths for multi-core platforms shared with other software components, under the constraint that the image processing performance may not decrease, in order to guarantee sufficient throughput for the printer.

Océ wide format printer



Océ high performance cut-sheet printer

The assignment

Professional printing involves the high-speed processing of large volumes of data (hundreds of A4 images per minute or high throughput printing of wide format images of several meters wide). The datapath component of professional printers is responsible for the processing of these images. The datapath contains two consecutive pipelines to process this stream of data: the rip path that converts pdf input files into bitmaps and the embedded print path that turns bitmaps into firing patterns for the inkjet print heads. The goal of this assignment is to investigate the possibility to implement the embedded print path for wide format printers on a multi-core platform. Such a multi-core implementation will cause resource sharing (processors, caches, memories, communication bandwidth) among the image processing steps in that pipeline, that can influence the throughput and thereby the processed image data per minute. The ambition is to determine before the full integration of the image processing pipeline on a multi-core platform, whether it can meet the given performance requirements. One challenge is that the platform may be shared with other software. Therefore the assignment is to model the temporal behavior of the image processing steps and to model their contention for shared resources in the platform. This assignment involves amongst others:

- Modelling of the temporal behavior of the image processing steps and the multi-core platform, including the relevant shared resources, using discrete event simulation.
- Definition of a sound contention model for the image processing steps in the presence of other software and verification of this contention model by performing measurements
- Performance prediction for the image processing steps, using the discrete event simulation of the image processing pipeline and one or more platform instantiations.

Further steps could include the optimization of the processing pipeline for a specific platform and a design space exploration of suitable alternative platforms components.

You can start after the summer vacation (i.e., after August 29) and will work in close cooperation with the Océ stakeholders and with ESI researchers. The assignment will be hosted by Océ Technologies in Venlo. Since a significant part of the assignment involves discrete event simulation and measuring the performance, we expect a solid knowledge of the C programming language. Experience with discrete-event-simulation is considered positive.

More information

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