electronics for embedded systems

static gates
complex gates in weak logic (pseudo-nmos)

- weak logica → **low** levels: design!
  
  \( (\text{high level always } V_+) \)

- lowest level: conduction through "longest" path
  
  and no parallel path

- current through all transistors equal

- requirement: \( v_{\text{out}} = v_k = \sum_{i=1}^{k} v_{d\text{s}_i} \leq V_{\text{OL}} \)

- body-effect of the nmos-transistors:
  all source voltages \( \leq V_{\text{OL}} \) → little body-effect

- region: pmos-transistor: \( v_{sbp} = 0 \) no body-effect
  
  \( v_{gs_p} = -V_+ < V_{tpo}; v_{gd_p} = -v_{\text{out}} > V_{tpo} \) → in saturation

- region: nmos-transistors:
  
  \( v_{gd_i} = V_{IH} - \sum_{j=0}^{i} v_{d\text{s}_j} > V_{IH} - V_{OL} > V_{teo} \) → out of saturation
complex gates in weak logic (pseudo-nmos)

the current through each nmos transistor is equal to the current through the pmos transistor: addition of these relations yields:

$$\frac{2}{\beta_{n_k}} i = \frac{\beta_p}{\beta_{n_k}} (V_+ + V_{tpo})^2 = (V_{IH} - V_{tno} - v_{k-1})^2 - (V_{IH} - V_{tno} - v_k)^2$$

$$\frac{2}{\beta_{n_{k-1}}} i = \frac{\beta_p}{\beta_{n_{k-1}}} (V_+ + V_{tpo})^2 = (V_{IH} - V_{tno} - v_{k-2})^2 - (V_{IH} - V_{tno} - v_{k-1})^2$$

$$\frac{2}{\beta_{n_2}} i = \frac{\beta_p}{\beta_{n_2}} (V_+ + V_{tpo})^2 = (V_{IH} - V_{tno} - v_1)^2 - (V_{IH} - V_{tno} - v_2)^2$$

$$\frac{2}{\beta_{n_1}} i = \frac{\beta_p}{\beta_{n_1}} (V_+ + V_{tpo})^2 = (V_{IH} - V_{tno} - v_0)^2 - (V_{IH} - V_{tno} - v_1)^2$$

$$\sum_{j=1}^{k} \frac{2}{\beta_{n_j}} i = (V_+ + V_{tpo})^2 \sum_{j=1}^{k} \frac{\beta_p}{\beta_{n_j}} = (V_{IH} - V_{tno} - v_0)^2 - (V_{IH} - V_{tno} - v_k)^2$$

$$v_k \leq V_{OL} \rightarrow \sum_{j=1}^{k} \frac{1}{\beta_{n_j}} \leq \frac{(V_{IH} - V_{tno})^2 - (V_{IH} - V_{tno} - V_{OL})^2}{\beta_p (V_+ + V_{tpo})^2}$$

identical nmos transistors have to be $k$ times wider, than the nmos transistor of an inverter with the same requirements
weak logic in cmos: pseudo-nmos nor

for static cmos pla's: pseudo-nmos

• weak logic: levels!
• dissipation in static behavior!

\[ V_{ds_{n}} < V_{OL} < v_{gs_{n}} - V_{tno} \rightarrow \text{nmost out of sat.} \]
\[
\begin{align*}
\text{i} & = \frac{\beta_{n}}{2} \left[ 2(V_{IH} - V_{tno}) v_{out} - v_{out}^{2} \right] \\
\end{align*}
\]
\[
\begin{align*}
v_{sd_{p}} & = V_{+} - v_{out} \quad \text{no body-effect!} \\
v_{sg_{p}} & = V_{+} \\
v_{out} & < - V_{tpo} \quad \text{pmost in saturation} \\
\end{align*}
\]
\[
\begin{align*}
i & = \frac{\beta_{n}}{2} (V_{+} + V_{tpo})^{2} \quad \text{no body-effect!} \\
\end{align*}
\]
\[
\begin{align*}
v_{out}^{2} - 2(V_{IH} - V_{tno}) v_{out} + \frac{\beta_{p}}{\beta_{n}} (V_{+} + V_{tpo})^{2} & = 0 \\
\end{align*}
\]
\[
\begin{align*}
\frac{\beta_{n}}{\beta_{p}} & \neq \frac{W_{n}}{L_{n}} \frac{L_{p}}{W_{p}} \\
\end{align*}
\]
complementary logic

• complementary logic is strong logic
  - output always connected to one "strong" node (e.g. a supply voltage) or floats ("tristate")
  - pull-up and pull-down network never have both a conducting path to a strong node,
  - safe and without drawbacks:
    either the pull-down or the pull-up network has a conducting path to a strong node
• pull-up and pull-down networks are obtained:
  - with series-parallel networks:
    by replacing all "series" by "parallels" and all "parallels" by "series"
  - with planar * networks by dualisation
  - by using switching theory
  - by designing pass network

* planar means that the network can be drawn without crossing lines
complementary logic with “s-p” networks

the simplest method to complementary networks works only if one the two is available as a series-parallel network (there always exist an equivalent series-parallel network!)

exclusivity principle: if there is a conducting path in the pull-up network the pull-down network should not conduct
complementary logic with “planar” network

if "planar", pull-up and pull-down network can be each others "dual"

exclusivity principle:
when there is a conducting path in the pull-up network there should be none in the pull-down network

each path in one network corresponds with a cut in the complementary network
non-dual complementary networks

pull-up and pull-down network do not have to be each other's dual: every logically equivalent pass network yields the same combinatorial behavior (but not always the same performance: speed, size, regularity etc.)

still the "exclusivity principle", but now achieved with logic synthesis!
cmos design

• no worry about levels in static cmos-gates:
  - always asymptotically equal to strong levels

• concentrate on speed / power
  - rc-models
  - transistor sizing
  - elmore models for long series

• noise properties
  - inversion voltage

By definition, the output voltage is equal to the input voltage at the switching threshold.

\[ V_{in} = V_{out} = V_{th} \]  

(7.30)

It is obvious that the two parallel nMOS transistors are saturated at this point, because \( V_{GS} = V_{DS} \). The combined drain current of the two nMOS transistors is

\[ I_D = k_n \left( V_{th} - V_{T,r} \right)^2 \]  

(7.31)

Thus, we obtain the first equation for the switching threshold \( V_{th} \),

\[ V_{th} = V_{T,n} + \sqrt{\frac{I_D}{k_n}} \]  

(7.32)

Examination of the p-net in Fig. 7.10 shows that the pMOS transistor M3 operates in the linear region, while the other pMOS transistor, M4, is in saturation for \( V_{in} = V_{out} \). Thus,

\[ I_{D3} = \frac{k_p}{2} \left[ 2(V_{DD} - V_{th} - |V_{T,p}|)V_{SD3} - V_{SD3}^2 \right] \]  

(7.33)

\[ I_{D4} = \frac{k_p}{2} \left( V_{DD} - V_{th} - |V_{T,p}| - V_{SD3}^2 \right) \]  

(7.34)

The drain currents of both pMOS transistors are identical, i.e., \( I_{D3} = I_{D4} = I_D \). Thus,

\[ V_{DD} - V_{th} - |V_{T,p}| = 2 \sqrt{\frac{I_D}{k_p}} \]  

(7.35)

This yields the second equation of the switching threshold voltage \( V_{th} \). Combining (7.32) and (7.35), we obtain

\[ V_{th} = \frac{V_{T,n} + \sqrt{\frac{k_p}{2} \left( V_{DD} - |V_{T,p}| \right)}}{1 + \frac{1}{2} \frac{k_p}{k_n}} \]  

(7.36)

Now compare this expression with the switching threshold voltage of the CMOS inverter, which was derived in Chapter 5.
the simplest gate
A NAND-gate

<table>
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<tr>
<th>in₁</th>
<th>in₂</th>
<th>out</th>
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<tbody>
<tr>
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<td>low</td>
<td>high</td>
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<td>high</td>
<td>high</td>
<td>low</td>
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</tbody>
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Diagram of a NAND-gate:

- **Input 1 (in₁):**
  - Low
  - High

- **Input 2 (in₂):**
  - Low
  - High

- **Output (out):**
  - High
  - High
  - High
  - Low

Diagram illustrates the connections and logic of a NAND-gate with input 1 (P) and input 2 (N), leading to the output (out).