for static memory operation
there has to be more than
one possible static state:

\[ f[f(v)] = f^2(v) = v \]

\[ f(v) = f^{-1}(v) \]

the static transfer characteristic of the "identity" is \( f[f(v)] \)

the static equations have to have more than one solution
static solutions

\[
f[f(v)] = f^2(v) = v
\]

\[
f(v) = f^{-1}(v)
\]

\[v = V_+ \rightarrow v \geq V_{IH} \rightarrow f(v) \leq V_{OL} < V_{IL} \rightarrow V_{OH} \leq f[f(V_+)] \leq V_+
\]

the static equations have to have more than one solution
the static solutions have to have more than one solution
condition for bistability

\[ f[f(v)] = v \]
The condition for bistability is given by:

\[
\left[ \frac{d\{f[f(v)]\}}{dv} \right]_{v=v_{inv}} = \left[ \frac{df(v)}{dv} \right]_{v=v_{inv}}^2 > 1
\]

If

\[
\left[ \frac{df}{dv} \right]_{v=v_{inv}} < -1
\]

then a circuit with cross-coupled invertors has at least three static states.
the solution at $v = v_{\text{inv}}$

around $v = v_{\text{inv}}$ dynamic solution $\rightarrow i_{p,u} = i_{p,d} + C \frac{dv_2}{dt}$

the nmos transistor in saturation

$$G(V_+ - v_2) = \frac{\beta e}{2} (v_1 - V_{\text{te}})^2 + C \frac{dv_2}{dt}$$

nmos in verzadiging

$v_1 - V_{\text{tno}} = v_2$
the solution at $v = v_{\text{inv}}$

around $v_{\text{inv}}$:

attention: $G$ is non-linear!

locally linearised:

$$g(v_2 - v_{\text{inv}}) = \beta_e (v_{\text{inv}} - V_{\text{te}})(v_1 - v_{\text{inv}}) + C \frac{dv_2}{dt}$$

$$g(v_1 - v_{\text{inv}}) = \beta_e (v_{\text{inv}} - V_{\text{te}})(v_2 - v_{\text{inv}}) + C \frac{dv_1}{dt}$$

$$g(v_2 - v_1) = -\beta_e (v_{\text{inv}} - V_{\text{te}})(v_2 - v_1) + C \frac{d(v_2 - v_1)}{dt}$$

$$\begin{cases}
G(V_+ - v_1) = \frac{\beta_e}{2} (v_2 - V_{\text{te}})^2 + C \frac{dv_1}{dt} \\
G(V_+ - v_2) = \frac{\beta_e}{2} (v_1 - V_{\text{te}})^2 + C \frac{dv_2}{dt}
\end{cases}$$

slope co-efficient $g = \frac{dG}{dv_2} < 0$

a differential equation in $v_2 - v_1$
the solution at $v = v_{\text{inv}}$

solution:

$$v_2(t) - v_1(t) = (v_2(0) - v_1(0)) \exp\left(1 + \frac{\beta_e}{g} (v_{\text{inv}} - V_{\text{te}}) \right) \frac{g t}{C}$$

because

$$\left[ \frac{\partial v_{\text{out}}}{\partial v_{\text{in}}} \right]_{v_{\text{in}} = v_{\text{inv}}} = \frac{\beta_e}{g} (v_{\text{inv}} - V_{\text{te}}) = f'(v_{\text{inv}})$$

$$v_2(t) - v_1(t) = \Delta v(0) \exp\left((f'(v_{\text{inv}}) + 1) \frac{g t}{C}\right)$$

the gain at the inversion point ($f'(v_{\text{inv}})$) is smaller than $-1$!
the potentials $v_1$ en $v_2$ diverge further and further

$$g(v_2 - v_1) = -\beta_e (v_{\text{inv}} - V_{\text{te}})(v_2 - v_1) + C \frac{d(v_2 - v_1)}{dt}$$

this solution is called metastable.
the metastable state

- without noise:
  how long does it take until \( v_2(t_s) - v_1(t_s) = \Delta v_s \) if \( v_2(0) - v_1(0) = \Delta v \)

  \( \Delta v_s \) small enough for linear approximation

  \[
  v_2(t) - v_1(t) = \Delta v \exp\left(\frac{\beta_e (v_{\text{inv}} - V_{\text{teo}}) - g}{C} t\right)
  \]

  \[
  \rightarrow t_{v_2 - v_1 = \Delta v_s} = \frac{C}{\beta_e (v_{\text{inv}} - V_{\text{teo}}) - g} \ln \frac{\Delta v_s}{\Delta v}
  \]

  answer: arbitrarily long!

- with noise:
  noise does not prevent the metastable state
condition for bistability

\[
\left[ \frac{d\{f[f(v)]\}}{dv} \right]_{v=v_{inv}} = \left[ \frac{df(v)}{dv} \right]_{v=v_{inv}}^2 > 1
\]

if \[-1 < \frac{df}{dv} \bigg|_{v=v_{inv}} < 1\]

then a circuit with cross-coupled invertors has at least three static states.
the solution at $v = v_{inv}$

\[
v_2(t) - v_1(t) = (v_2(0) - v_1(0)) \exp\left(1 + \frac{\beta_e}{g} (v_{inv} - V_{te}) \right) \frac{g t}{C}
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because

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\left[ \frac{\partial v_{out}}{\partial v_{in}} \right]_{v_{in}=v_{inv}} = \frac{\beta_e}{g} (v_{inv} - V_{te}) = f'(v_{inv})
\]

\[
v_2(t) - v_1(t) = \Delta v(0) \exp\left((f'(v_{inv})+1) \frac{g t}{C}\right)
\]

the gain at the inversion point ($f'(v_{inv})$) is smaller than -1!

the potentials $v_1$ en $v_2$ diverge further and further

\[
g(v_2 - v_1) = -\beta_e (v_{inv} - V_{te}) (v_2 - v_1) + C \frac{d(v_2 - v_1)}{dt}
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$$g(v_2 - v_1) = -\beta e (v_{\text{inv}} - v_{\text{te}})(v_2 - v_1) + C \frac{d(v_2 - v_1)}{dt}$$

this solution is called metastable.
for "latching" is needed
- 2 inverting elements
- cross coupling
- differential gain $< -1$
at $v_{inv}$

switching by:
1. breaking the coupling
switching of a latch

for "latching" is needed
- 2 inverting elements
- cross coupling
- differential gain $< -1$
at $v_{\text{inv}}$

switching:
1. breaking the coupling
2. annihilate inversion
switching of a latch

for "latching" is needed
- 2 inverting elements
- cross coupling
- differential gain $< -1$
  at $v_{\text{inv}}$

inverting operation annihilated

$s$ is high
dynamic memory

dynamic memory "remembers" by isolating charge at a node ("weak or floating nodes")
**dynamic nmos memory element**

leakage:
- bottom: 0.25 fA/\(\mu\)m²
- side: 4 fA/\(\mu\)m²

\[ C_{st} = C_{junction} + C_{gate} = (0.02 + 0.03) \text{ pF} \]

\[ \frac{dV}{dt} \approx \frac{I_{\text{leak}}}{C_{st}} \approx 6 \frac{V}{\text{sec}} \]

\( V_+ = 5V \quad V_{teo} = 1V \)

\( V_{IH} = 3V \)

\( T_H \approx 166 \text{ msec} \)

\( I_{\text{leakage}} = 0.3 \text{pA} \)

\( T_H \) decreases exponentially with the temperature!

At 85°C: 60x larger leakage current!
dynamic memory element in cmos

$\begin{align*}
  v_{in} &= V_+ \\
  v_{st}(0) &= 0 \\
  v_{st} &= V_+ \left(1 - e^{\frac{-t}{R_sC_{st}}}\right)
\end{align*}$

$\begin{align*}
  v_{in} &= 0 \\
  v_{st}(0) &= V_+ \frac{-t}{R_sC_{st}} \\
  v_{st}(t) &= V_+ e^{\frac{-t}{R_sC_{st}}}
\end{align*}$
dynamic memory element in cmos

\[ \text{asymptotic level depends on } \frac{G_1}{G_2} \text{ ratio} \]
charge sharing

\( S \) non conducting

\[ Q_{\text{tot}} = C_1 v_1 + C_2 v_2 \]

\[ v = \frac{Q_{\text{tot}}}{C_1 v + C_2 v} = \frac{C_1 v_1 + C_2 v_2}{C_1 + C_2} \]

so \( v_2 = 0 \):

\[ v = \frac{1}{1 + \frac{C_2}{C_1}} v_1 \]

\[ v_1(t > t') = \frac{V_+ - V_{te}}{1 + \frac{C_2}{C_1}} = v_2(t > t') \]
memories

ram: random-access-memory can be read and written fast
- static (eccles-jordan cells)
  hold time unlimited if the supply voltage stays
- dynamic (charge storage)
  "refresh" (e.g. dummy read)

bits, bytes, halfwords, words, double words

access time, cycle time

adressing, adres decoding
static memory cell

bit

word

\( T_3 \)

\( T_5 \)

\( T_6 \)

\( T_4 \)

\( T_1 \)

\( T_2 \)
reading and writing

both, for writing as well as reading the wordline must be high

writing:
1) charging of one of the bit lines
2) charging of the word line

suppose \( \overline{\text{bit}} = 0 \rightarrow T_1 \) must be off

\( \beta_6 \) relatively low with respect to \( \beta_4 \)

reading:
1) precharging the bit lines
2) charging the word line

\( \beta_4 \) relatively low with respect to \( \beta_2 \)
variants

only one bit line

"multiport-memory"
2 cells written or read simultaneously
static memory cell
dynamic memory cells

static principle: the capacitances are being kept by the pull-ups

dynamic principle: levels kept by isolating capacitive nodes
dynamic three-transistor cell

- State of the cell: charge on $C$
  - Writing:
    1) Put $b_{\text{in}}$ at the right level
    2) Let $T_3$ conduct
  - Reading:
    1) $b_{\text{out}}$ charged
    2) Let $T_4$ conduct

- Hold time: a few milliseconds
- Refresh: read and write back

- No strict $\beta$ ratios
- Low dissipation
three-transistor cell

\[ b_{in} \]

write

\[ C_g \]

read

\[ b_{out_1} \]

read\(_2\)
one-transistor-cell

writing: bit and word line high

reading = detecting

\[
\frac{C}{C + nC_b}(V_c)
\]

charge transfer ratio

\(n = \text{number of cells at the bit line}\)