analysis and synthesis of electronic circuits

5HH10
course 2006
Ralph Otten
about this lecture

- originally: numerical methods
- consideration: why not network simulation?
- decided: the inner works of SPICE
  - SPICE is available!
  - useful for calculating circuits in 5HH00 and beyond
  - recognize and understand spurious errors
- assessment: half a lecture analysis of electronic circuits
- other half: synthesis of electronic circuits (i.e. chips)
  - an idea of chips and their making
  - back-end automation (i.e. mask synthesis)
    - flows
- written exam in June

**today: chip-intro**
a closer look at a chip

- a square chip of pure silicon (Si)
- many chips are built on a single wafer

- chips are packaged using gold wires; the connections are made

- wafer: 14 inch; it will be cut into a hundreds chips
the ‘layout’ of a chip

• the pattern determines the functionality:
  - transistors
  - Cu/Al wires (up to 9 layers)
  - contact between layers

transistor: crossing between red and green.
contact
blue = metal 1 Cu/Al wire
bonding pads for gold wires
structure on a chip: many levels

- 5th level wire
- 4th level wire
- 3rd level wire
- 2nd level wire
- 1st level wire
- Transistor
- Silicon substrate
the scale of a chip

- the largest chips are approximately 1.5 x 1.5 cm (0.5 by 0.5 inch), still smaller than a penny!

- at this moment, we design:
  - up to 1,000,000,000 transistors on a chip.
  - switch some transistors over 3,000,000,000 times per second.
  - put over 1 kilometer (0.7 miles) over wires on a chip.
imagine that a wire on the chip is the size of a road, and roads are shoulder-to-shoulder for 7 levels,

then a transistor has the size of a car... and the chip covers most of Western Europe...
so... what is this transistor?

a switch!

- Every transistor either conducts electricity, or it doesn't.
let's take a hike on the beach...

thin layer of water on the sand.

when you stepped here the layer of water disappears!
the water sinks in the spaces between the grains of sand!

- originally, the grains of sand on the beach are well aligned: between the grains there is hardly any space for water.
- a thin layer of water is on top of the sand.

- applying pressure will distort this perfect arrangement: space will occur between the grains.
- this space absorbs the layer of water.
so what's the analogy between the step on the beach and a silicon transistor?

- water = electrons
- sand grains = silicon atoms
- apply 3 contacts: source, drain and gate
- pressure = gate voltage

- no voltage on gate: no flow of electrons between source and drain.
  - the switch is OFF

- apply a voltage on the gate: electrons can flow between source and drain.
  - the switch is ON
MOS history: basic patents by Lilienfeld

Julius Edgar Linienfeld (1881-1963)

- a real inventor:
  - new x-ray tube
  - loudspeaker,
  - spark plug,
  - pupillograph, camera, elastic fabrics
  - electrolytic capacitors
  - mos transistor!
semiconductor work at Bell Labs

- Linienfeld never implemented his devices on Silicon; the inventions were "forgotten"
- 1940: Ohl develops the silicon PN Junction
- 1945: Shockley's laboratory established
- 1947: Bardeen and Brattain create point contact transistor (U.S. Patent 2,524,035)
- 1951: Shockley develops a junction transistor manufacturable in quantity (U.S. Patent 2,623,105)
the birth of ‘Silicon Valley’

- 1950s: Shockley moves back to Palo Alto, Silicon Valley
  - starts company and hires Gordon Moore, Robert Noyce
- 1954: the first transistor radio
- 1957: after a dispute with Shockley, Robert Noyce leaves Shockley Labs to form Fairchild with Jean Hoerni and Gordon Moore
- 1958: Hoerni invents technique for diffusing impurities into Si to build planar transistors using a SiO₂ insulator
- 1959: Noyce develops first true IC using planar transistors, back-to-back PN junctions for isolation, diode-isolated Si resistors and SiO₂ insulation with evaporated metal wiring on top.
the integrated circuit

• 1959: Jack Kilby, working at TI, dreams up the idea of a monolithic “integrated circuit”
  - components connected by hand-soldered wires and isolated by “shaping”, PN-diodes used as resistors (U.S. Patent 3,138,743)

![Diagram from patent application](image)
integrated circuits

- 1961: debut of commercial logic ic's ($50 in quantity)
the first computer-aided design for ic's

- 1967: Fairchild develops the “Micromosaic” IC: a semicustom chip in which programmable layer of interconnect: simple tools evolve to help design it.

- 1968: Noyce and Moore leave Fairchild to start Intel
- other 'Fairchildren': National Semiconductor, AMD, Signetics.
many transistors: Moore's law

• Gordon Moore in 1964:
  - the integration density on an IC with double every 18 month

• this has be true for almost 40 years
• ... and will probably be true for at least another 10 years.
many transistors: Moore’s law

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• this has be true for almost 40 years
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Moore's law

The growth rate of chip complexity will be proportional to the achieved complexity to date.

\[ \frac{dN}{dt} \propto N \]

Proportionality constant, "Moore exponent m", 0.2 for processors, and 0.4 for memory.

\[ N = \text{numerical complexity of the module (e.g. the chip)} \]
Rent's rule

The growth rate of the terminal count with the complexity of the module will be proportional to the average number of terminals per submodule.

\[ \frac{dT}{dN} \propto \frac{T}{N} \]

\[ T(N) = \text{the number of terminals of a module with numerical complexity } N \]

\[ N = \text{numerical complexity of the module (e.g. the chip)} \]

[Landman, Russo, 1971]
The reduction rate of device sizes will be proportional to the achieved device size.

[Status2000, ICE, 2000]

Proportionality constants are pretty close in value and will be called the "process exponent p".

\[ \frac{dL}{dt} \propto -L \]
feature size
feature size
feature size
feature size
feature size
feature size
classifications: fabrication perspective

- off-the-shelf
- programmable
- semicustom (master image)
- full custom
classifications: designer's perspective

- full custom
- semicustom (master image)
  - off-the-shelf
    - component
    - field programmable
  - programmable
    - mask programmable
  - sea-of-gates
    - gate array
gate array
sea-of-gates (channelless array)
PHILIPS microprocessor
macrocell assembly
polycell versus gate array

- rows, longitudinally aligned
- variable width channels
- bonding pads as required

- rows of identical cells
- fixed width channels
- fixed footprint
polycell layout style
power pc processor
choosing a style

cumulative cost

semi-custom

full custom

field programmable

number of products produced
choosing a style

cumulative cost vs. number of products produced

- full custom
- semi-custom
- field programmable
the output: layout

mask = 2-block partition of the plane ("opaque", "transparent")
("write", "no-write")

layout = specification of "masks"

= files of rectangles with a color
design rules
technology constraints (design rules)

- technology rules are translated into design rules
- the design rule set is the interface between designer and foundry
- rules are simplified and often on the safe side
- certain rules are always assumed!

- for synthesis we distinguish
  - numeric rules
    - small total area
    - reduction to "pitches"
      R1: wire width per layer
      R2: wire separation per layer
      R3: contact rules

- structural rules
incidence structures (net lists)

modules:
- M supermodule of $m_1$, $m_2$ and $m_3$
- $m_1$, $m_2$, and $m_3$ submodules of M

pins $p_1$ ... $p_{13}$
relating nets with modules

also:
a bipartite graph,
"the potential graph"
$(M \cup N, P)$

local nets: $N_1$, $N_3$
global nets: $N_2$, $N_4$, $N_5$
rectangle constraint

- top down design
  - initially very little geometrical knowledge is available
  - stepwise refinement
    - postpone decisions to get as much information as possible
    - each decision adds knowledge to the next step or the other part
  - decompose the whole design task into subtasks
    - apply as much as possible the same approach to each part
      this produces true hierarchy:
      hierarchy = a set of hierarchies and leaf cells
    - special problems are treated by special dedicated routines

- flexibility
  - built-in capability to update the available information
    - fast optimization algorithms
    - easily adaptable configurations

- self fulfilling shape requirement

deviations contained in inset cells
layout design

functional specification

silicon compilation

layout design

technology file (design rules)
traditional task decomposition

- placement
  - partitioning
    - dividing the netlist into smaller parts
      - controlling the "sizes" of the parts and
      - the number of interconnections between them
  - floorplanning
    - determining the relative positions of the parts
      - and their target shapes
  - detailed placement
    - manipulating the position and orientation
      - of geometrically fixed modules in the netlist

- routing
  - global routing
    - determining wire congestion
      - on the basis of relative positions
  - detailed routing
    - determining the exact geometry
      - of the interconnections in the netlist