TELEVISION NOISE REDUCTION IC

Philips Semiconductors, Eindhoven, The Netherlands

ABSTRACT
A noise reduction IC for consumer television has been designed. The IC contains a spatial filter for Gaussian noise and a temporal filter for clamp noise. Both filters automatically adapt to the noise level.

INTRODUCTION
Since TV sets are often used in areas where the reception conditions are not optimal, inclusion of a noise reduction filter in the receiver adds an attractive feature. Spatial noise filters can be economically implemented in silicon, as has been mentioned in an earlier paper [2]. However, specific types of noise, such as clamp noise and low-frequency interference, needs a temporal filter for effective suppression [3,4]. Up to now, temporal filters have only been suitable for high-end applications, since they require an (expensive) field memory. This paper describes how a new algorithm for economic implementation of temporal noise filtering has been developed, and how this algorithm has been used in the design of a new IC for TV noise filtering. The IC includes a circuit for noise level estimation and combines spatial and temporal noise filtering. This mixture of techniques is very effective against both Gaussian and clamp noise and performs very favourably at varying noise levels.

THE ALGORITHM
The newly developed IC contains a locally adapting 2-D recursive spatial filter and a noise estimation circuit that have also been introduced in a separate IC-design [1,2]. A new element in the current design is the temporal noise filter. It temporally filters average pixel values of line segments. Order statistics is used to determine a stationary line segment, and to calculate a DC-correction for each line of pixels, which is then applied to all pixels on that line. This effectively removes the very low frequencies of the noise spectrum, e.g. clamp noise. The (recursive) filtering of average values rather than pixel values, reduces the memory capacity of the temporal delay elements in the filter with three orders of magnitude. This enables the use of a cost-effective embedded memory for the field-time delays, and prevents blurring of picture detail. Figure 1 shows the circuit. (The algorithm will be described more elaborately in the full paper). The noise level estimation circuit [1] measures the noise in the active video to prevent estimation error due to clean blanking levels inserted by e.g. home recorders. The relation between the noise estimate and the filter settings can be adapted to the preference of the user.

THE VLSI DESIGN
The noise reduction IC filters 8-bit digitized luminance and colour difference signals, and has an output accuracy of 10 bits. The preference of the user is programmed via an I2C-bus interface. The sampling clock is generated by an embedded line-locked phase-locked loop operating at 13.5 MHz. The IC includes a split-screen demonstration mode, analogue interface and integrated clamp, pre-and post-filters. The noise filter apertures for luminance and chrominance are independently programmable across a wide range. The IC has switchable line delay (PAL) and line-comb functions (NTSC), and a low-power standby mode. Further key data is presented in Table 1. Figure 2 shows the lay-out of the IC.

THE PERFORMANCE
The noise reduction IC yields a gain on Gaussian noise of approximately 3 dB. The temporal noise filter of the IC realizes 6 dB gain in LF-noise, in particular on clamp noise. These gain figures are obtained in a large range of S/N ratios because of the noise estimator on board the IC. A subjective evaluation [1] showed that the gain on Gaussian noise can be increased to almost 6 dB by cascading the new IC design with a classical [3,4] motion adaptive temporal noise filter.

CONCLUSIONS
A unique, automatically adapting spatio-temporal noise filter for television application was designed and realized in silicon with the help of a new algorithm. This noise reduction IC yields a gain on Gaussian noise of approximately 3 dB. The temporal noise filter on board the IC realizes some 6 dB gain in LF-noise, in particular on clamp noise. The interfaces of the new chip match existing chip sets available on the market for high quality television.

1. This IC is commercially available as SAA4986
REFERENCES


Table 1 Key IC data

<table>
<thead>
<tr>
<th>Process</th>
<th>CMOS 0.8 µ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size</td>
<td>53 mm²</td>
</tr>
<tr>
<td># transistors</td>
<td>300,000</td>
</tr>
<tr>
<td>Memory</td>
<td>36.5 kbit</td>
</tr>
<tr>
<td>Dissipation</td>
<td>0.8 W (5V, 13.5 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>SDIL42</td>
</tr>
<tr>
<td>I/O</td>
<td>Analogue</td>
</tr>
<tr>
<td>Data clock</td>
<td>13.5 MHz</td>
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Fig.1 Block diagram of the temporal noise reduction filter as used in the new IC

Fig.2 Lay-out of the noise reduction IC for television