### EFFICIENT NN W/O MULTIPLIERS

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Sebastian Vogel NXP - CTO Automotive System Innovations MARCH 2022



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#### EMBEDDED AI RESEARCH SCIENTIST, SEBASTIAN VOGEL

- Sebastian Vogel
  - PhD in "Efficient Processing of DNNs" from RWTH Aachen, Germany
  - 2016-2021 with Bosch Corporate Research, Renningen, Germany
    - Quantization, Hardware-Accelerator Architectures for DNNs, NAS
  - At NXP since Feb. 2021 as research scientist for Embedded AI
    - Hardware-aware Neural Architecture Search, Quantization
  - Presentation mostly shows work published while at Bosch Research
- NXP department: CTO Automotive System Innovations ('R&D')
  - Scouting & analysing AI research (in-house, via university collaborations)
  - Translate recent SOTA to NXP requirements & research projects
  - Small impactful projects with opportunities for student assignments



Bosch Research in Renningen (Research Campus) \*



NXP headquarters in Eindhoven (High Tech Campus) \*\*



<sup>\*\*</sup> source NXP Headquarters: https://www.nxp.com/company/about-nxp/worldwide-locations/netherlands:NETHERLANDS

#### PORTFOLIO OF NXP

- Functionality:
  - Compute
  - Connectivity
  - HMI

- Data:
  - Radar
  - UWB
  - Analytics
  - Vision

- Applications:
  - Automotive
  - IoT/edge
  - Industrial automation
  - Drones

#### For AI deployment:

- Applications
- Chips
- Constraints
- → different requirements on neural network architectures







- NXP CTO ('R&D') Automotive System Innovations (ASI)
  - Prototyping systems with NXP solutions, e.g.:
  - Radar, AI/ML 'brain', Network
  - In-house & collaborations









Slide courtesy: Willem Sanberg willem.sanberg@nxp.com

#### EFFICIENT NNS WITHOUT MULTIPLIERS OVERVIEW

- Quantization of Neural Networks w/o Multipliers
  - Self-supervised quantization of pre-trained DNNs
  - Logarithmic quantization at arbitrary base
  - Bit-shift-based quantization



## Quantization of DNNs (w/o Multipliers) **Self-supervised quantization** Logarithmic number representation **Bit-shift-based quantization**



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#### SELF-SUPERVISED QUANTIZATION OF PRE-TRAINED NEURAL NETWORKS DOES NOT REQUIRE LABELLED TRAINING DATA

- Quantizing pre-trained neural networks, i.e., determining the quantization step size  $\alpha$ 
  - Without the need for labeled training data through self-supervised quantization<sup>[7]</sup>
  - Unlabeled calibration enough

Option 1: Minimize the squared QE  $\alpha = argmin\left(y_{\Delta}^{\left(l\right)^{2}}\right)$  Option 2: Minimize squared propagated quantization error  $\alpha = argmin\left(y_{p\Delta}^{(l)^2}\right)$ 

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[7] Vogel et al., Self-Supervised Quantization of Pre-Trained Neural Networks for Multiplierless Acceleration, DATE 2019

#### SELF-SUPERVISED QUANTIZATION OF PRE-TRAINED NEURAL NETWORKS

<ul> <li>8bit quantization (per-tensor) of activations only Classing</li> </ul>							ation Semantic Segmentation					
										)		
Quantization	VGG16		ResNet50		InceptionNet		Dilated Model		FCN8s			
	top-1 <sup>+</sup>	top-5**	top-1	top-5	top-1	top-5	mloU§	pix.acc.#	mloU	pix.acc.		
Calibration samples	100							36	36			
Float32 baseline	69.58	89.04	72.99	90.93	75.61	92.48	55.63	92.85	66.48	94.65		
$y_q$ max abs (naïve)	66.36	88.82	64.75	86.69	0.00	0.02	51.70	91.14	64.68	93.41		
$y_q$ min MSE (Opt. 1)	68.51	88.79	70.08	88.95	69.66	89.40	54.23	92.00	65.04	93.29		
$y_q$ min propQE (Opt. 2)	69.09	88.97	71.31	90.61	73.89	91.67	55.65	92.79	66.49	94.46		
propQE vs baseline	-0.49	-0.07	-1.68	-0.32	-1.72	-0.81	+0.02	-0.06	+0.01	-0.19		

Float 32bit



[4]

Linear 8bit (params & act.)



+ Top-1 accuracy: % of correctly classified labels ++ Top-5 accuracy: % of correct label within first 5 predicted labels § mIoU: mean intersection over union # pix.acc.: mean overall pixel accuracy

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# Quantization of DNNs w/o Multipliers

Self-supervised quantization

Logarithmic number representation

**Bit-shift-based quantization** 





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#### FEW-BIT QUANTIZATION WITH ARBITRARY LOG-BASE IS A PROMISING APPROACH FOR PRESERVING PRE-TRAINED NETWORK ACCURACY

- As of 2018, few-bit-quantization lacked behind SOTA floating point training and resulted in complex training routines and hard to master training "ingredients"
- Quantization of pre-trained DNNs favorable
- CNN accelerators incorporate a considerable amount of multiply-accumulate (MAC) engines
- Reducing the bit-widths optimizes for power and memory requirements
- Adders and bit-shifts lead to considerably reduced area requirements compared to MACs



#### LOG-QUANT WITH ARBITRARY LOG-BASES INCORPORATES INTRINSIC PRUNING EFFECT [8]



• Logarithmic quantization incorporates an intrinsic pruning effect when choosing base a < 2 <sup>[8]</sup>

[8] Vogel et al., Efficient hardware acceleration of CNNs using logarithmic data representation with arbitrary log-base, ICCAD 2018



#### THE SAME OPTIMAL LOG-BASE IS FOUND FOR ALL LAYERS, MAKING A HW-IMPLEMENTATION LESS COMPLEX

- Optimal log-bases are determined by minimizing the propagated quantization error (propQE)
- Different optimal log-bases are found for weights and activations
- For ResNet50, the same optimal log-base is found in every layer
   → No HW-flexibility required for changing the log-base



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#### LOGARITHMIC QUANTIZATION OF CNNS WITH ARBITRARY LOG-BASE

- In ResNet50, the same optimal log-base is found in every layer
- In InceptionResNet, there are exceptions to this behavior, yet choosing a single optimal log-base for all layers achieves still considerably good results





#### LOG-BASED QUANTIZATION ACHIEVES COMPETITIVE RESULTS COMPARED TO LINEAR QUANT. ON SEVERAL DNN ARCHITECTURES

Logarithmic quantization of weights\* and activations at 5 bit



Linear 8bit



Logarithmic 5bit



<sup>+</sup> Top-1 accuracy: % of correctly classified labels
 <sup>++</sup> Top-5 accuracy: % of correct label within first 5 predicted labels
 § mIoU: mean intersection over union
 # pix.acc.: mean overall pixel accuracy

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\* per-tensor quantization and biases @8bit (linear) per-tensor

[4]

[4] Vogel, Design and implementation of number representations for efficient multiplierless acceleration of convolutional neural networks, PhD Thesis 2020

[4]

#### LOG-BASED MAC-ELEMENTS ARE COMPLEX BUT HAVE REDUCED INTERFACE BIT-WIDTHS

- Log-based number representations allow reducing the external bit-widths and therefore, optimize external bus and memory requirements
- Nevertheless, an implementation of a log-based MAC\*-element consists of more stages than its linear implementation



\* MAC – multiply-accumulate



#### ARE THERE WAYS TO ADDRESS THE DISCUSSED DOWNSIDES OF THIS LOG-BASED NUMBER REPRESENTATION?

- In the following, an alternate approach is presented addressing the drawbacks of log-based quantization with arbitrary log-base
  - Complex MAC-element implementation
  - Reduced accuracy on complex DNN architectures

Quantization	Bit- Width	VG top-1⁺	G16 top-5 <sup>++</sup>	ResN top-1	let50 top-5	Incept top-1	ionNet top-5	Dilateo mloU§	d Model pix.acc.#	FCN mloU	18s bix.acc.
Calibration samples	-	100						36		10	
lin-quant baseline	8	69.12	89.06	71.67	90.73	73.71	91.57	55.62	92.78	66.47	94.44
$w: \log_{2^{1/2}} y: \log_{2^{1/4}}$	5	68.46	88.36	66.89	87.08	64.65	85.55	54.83	92.65	66.05	94.39
log vs linear	-	-0.66	-0.70	-4.78	-3.65	-9.06	-6.02	-0.79	-0.13	-0.42	-0.05





# Quantization of DNNs w/o Multipliers

Self-supervised quantization

Logarithmic number representation

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- CNN accelerators incorporate a considerable amount of multiply-accumulate engines
- Fixed-point multipliers are considerably larger (wrt. silicon area) than shift-operations
- Shift-based operation
  - $\rightarrow$  logarithmically quantized weights (4bit)
- Note:

This approach uses linearly quantized activations and therefore, integrates standard input signals more easily





Quantization of weights (with bimodal distribution)
linear







- Quantization of weights (with bimodal distribution)
  - linear
  - "one-hot"





- Quantization of weights (with bimodal distribution)
  - linear
  - "one-hot"
  - "two-hot"



[4] Vogel, Design and implementation of number representations for efficient multiplierless acceleration of convolutional neural networks, PhD Thesis 2020

NO

#### LOG-BASED QUANTIZATION ACHIEVES COMPETITIVE RESULTS COMPARED TO LINEAR QUANT. EVEN ON COMPLEX DNN ARCHITECTURES

Log-based quantization (per-tensor) of

weights, biases<sup>\*</sup>, and activations<sup>\*</sup> Classification Semantic Segmentation **Dilated Model** Quantization **VGG16** InceptionNet FCN8s ResNet50 top-1<sup>+</sup> top-5<sup>++</sup> mloU<sup>§</sup> pix.acc.<sup>#</sup> mloU pix.acc. top-1 top-5 top-1 top-5 **Calibration samples** 100 36 10 lin-quant baseline 92.78 69.12 89.06 71.67 90.73 73.71 91.57 55.62 66.47 94.44 64.55 60.75  $w_a$  one-hot, 4 bit 86.76 46.36 72.11 37.77 49.52 90.13 92.10 63.85 *w<sub>a</sub>* **two-hot**, 8 bit 91.11 66.24 68.91 89.54 70.84 90.35 72.47 55.34 92.74 94.41 two-hot vs linear -0.83 -0.38 -1.24 -0.46 -0.28 -0.23 -0.21 +0.48-0.04 -0.03

Float32











+ Top-1 accuracy: % of correctly classified labels
 ++ Top-5 accuracy: % of correct label within first 5 predicted labels
 § mIoU: mean intersection over union
 # pix.acc.: mean overall pixel accuracy

\* activations, biases @8bit (linear)

[4]

[4] Vogel, Design and implementation of number representations for efficient multiplierless acceleration of convolutional neural networks, PhD Thesis 2020

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## MIXED-PRECISION LOG-BASED QUANTIZATION ALLOWS TO TRADE ACCURACY WITH THROUGHPUT AND NETWORK SIZE<sup>[9]</sup>



• Layers close to the network input are sensitive to one-hot quantization



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## MIXED-PRECISION LOG-BASED QUANTIZATION ALLOWS TO TRADE ACCURACY WITH THROUGHPUT AND NETWORK SIZE<sup>[9]</sup>



- Layers close to the network input are sensitive to one-hot quantization
- Layerwise selection allows to trade accuracy with throughput and resulting network size
- The configuration can be selected at run-time

#### BIT-SHIFT-BASED MAC-ELEMENTS WITH LINEAR QUANTIZATION FOR ACTIVATIONS OFFER FLEXIBLE MIXED-PRECISION COMPUTATION

- Implementations of bit-shift-based MAC<sup>\*</sup>-elements with "one-hot"/"two-hot" weights are less complex than log-based MAC-elements with arbitrary log-base
- Mixed-precision capability built in without the need for upper/lower nibble\*\* handling



\* MAC – multiply-accumulate

\*\* nibble - 4 bit



#### QUALITATIVE EVALUATION ON SEMANTIC SEGMENTATION

- Qualitative output of the dilated model for semantic segmentation on cityscapes
- Linear 8bit quantization (left), two-hot 8bit quantization (right), mutual diff. (bottom)



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[4] Vogel, Design and implementation of number representations for efficient multiplierless acceleration of convolutional neural networks, PhD Defense, Jan. 10, 2020

[4]

#### METHODS FOR QUANTIZING PRE-TRAINED NEURAL NETWORKS HAVE BEEN PRESENTED AND EVALUATED ON TWO APPROACHES FOR MULTIPLIERLESS EXECUTION OF DNNS

- We discussed a method for quantizing pre-trained neural networks without the need for fine-tuning on labeled training data  $y^{(l+1)} + y$ 
  - Minimizing the propagated quantization error

- Two approaches for few-bit quantization and multiplierless processing were discussed
  - Logarithmic number representation with arbitrary log-base
  - Mixed-precision log-based quantization ("one-hot"/"two-hot")





$$\alpha = argmin\left(y_{p\Delta}^{(l)^2}\right)$$

#### References

[1] Wang, et al. <u>HAQ: Hardware-Aware Automated Quantization with Mixed Precision</u>, CVPR2019

[4] Vogel, Design and implementation of number representations for efficient multiplierless acceleration of convolutional neural networks, PhD Thesis 2020

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[7] Vogel et al., Self-Supervised Quantization of Pre-Trained Neural Networks for Multiplierless Acceleration, DATE 2019

[8] Vogel et al., Efficient hardware acceleration of CNNs using logarithmic data representation with arbitrary log-base, ICCAD 2018

[9] Vogel et al., <u>Bit-Shift-Based Accelerator for CNNs with Selectable Accuracy and Throughput</u>, DSD 2019

#### AVAILABLE STUDENT PROJECT POSITIONS (INTERNSHIP & GRADUATION PROJECTS)

#### Automatic neural network quantization and deployment optimization

- optimizing neural networks through quantization and pruning
- taking multiple optimization criteria into account
- investigating options to learn how to quantize/prune neural networks
- automatically determining optimal SW deployment parameterizations for embedded devices

#### Hardware-aware NAS for next generation radar-based ADAS

- improving state of the art approaches on object classification with DNNs
- leveraging ML and NN-design know-how from other domains for Radar signal processing
- exploring NN designs that exploit Radar spectrum data, Radar target lists or a fusion of both
- optimizing simultaneously the deployment properties on target hardware and the task accuracy

#### AVAILABLE STUDENT PROJECT POSITIONS (INTERNSHIP & GRADUATION PROJECTS)

#### Transferring existing NAS methodologies to challenging embedded system tasks

- audio processing (noise cancelation, keyword spotting, etc.)
- battery management and battery health estimation
- predictive maintenance (e.g., anomaly detection)
- with the goal to derive insights on the trade-off between system requirements and task accuracy

#### Intelligent automated design & configuration of next generation DL-HW-accelerators

automatically optimizing configurable HW accelerators and co-adapting neural architectures
 especially focusing on quantization and sparsity features of HW-accelerators

#### Hardware-aware NAS for next generation hardware and software

- extending available hardware-aware NAS frameworks to new hardware targets;
- integrating said NAS frameworks with one of our existing training modalities;
- conducting extensive experiments in our training modalities.





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