

# Master Students

## (co-)supervised by Henk Corporaal

Eindhoven University of Technology (TU/e)

corporaal.org



Updated March 2020

### Notes:

- In the following list we use the abbreviations:
  - o ES: Embedded Systems Master at TU/e
  - o EE: Electrical Engineering Master at TU/e
- For Master students from the TUD (Technical University Delft), see the end of this file

### ***Graduated Master students, TU/e***

1. **Michel van Lier**, ES, January 2020  
Optimizing Neural Networks for Low-Complexity Channel Estimation  
With Zoran Zivkovic (Intel) and Alexios Balatsoukas
2. **Ruud Schellekens**, ES, Febr 2020  
Automatic Scheduling of Halide-HLS
3. **Joris Witteman**, EE, Nov 2019  
Energy efficient brain-controlled typing in 40nm
4. **Nick Bos**, EE, Nov 2019  
Mixed-Precision Neural Network Inference Acceleration on a Coarse Grain Reconfigurable Architecture  
With TUDresden.
5. **Floran de Putter**, EE, Oct 2019  
Mixed-precision TTA Accelerator for Binary Neural Networks
6. **Hein Breukers**, EE, Nov 2019  
Energy-Efficient EEG based Epileptic Seizure Classification using Neural Networks on an Embedded Platform

7. **Pim Hacking**, ES, Oct 2019  
Classification of Jetting Behavior based on Self-Sensing Piezo Actuators  
With OCE-CANON, Venlo
8. **Geert Linders**, ES, Aug 2019  
Compiler Vectorization for Coarse-Grained Reconfigurable Architectures
9. **Alejandro Heredia Cervantes**, ES, March 2019  
Efficient Mapping of EEG Algorithms on the CGRA architecture  
With Jos Huisken and Barry de Bruin
10. **Janek van Oirschot**, ES, March 2019  
Automatic generation of a fast peephole optimizer for LLVM  
With Microsoft Cambridge UK
11. **Jeroen Gubbels**, EE, February 2019  
Radiation measurement using COTS cameras  
Part of the PR3 rocket project (see pr3.space)
12. **Shihua Huang**, ES, February 2019  
Flexibility metric for processors
13. **Ian Zhang**, ES, December 2018  
Polly loop transformations using Machine Learning  
With TUBerlin
14. **Xin Xu**, ES 2018  
X-ray imaging  
With Philips Eindhoven
15. **Louis van Harten**, EE 2018  
Low cost radio interferometry  
Part of the PR3 rocket project (see pr3.space)
16. **Justing Brouwer**, ES 2018  
CGRA architecture generation
17. **Jeroen Biesbroeck**, ES, 2018  
CNNs for radar images  
With NXP
18. **Sander Walstock**, ES, 2018  
CGRA multiprocessor communication and synchronization
19. **Rick Veens**, ES 2018  
WCET estimation  
With SPACEBEL Liege, Belgium

20. **Guus Leijsten**, ES, 2018  
SIMD LLVM backend
21. **Joep Roebroek**  
Cognitive Neural Networks, ES, 2017
22. **Zhenyuan Liu**, ES, 2017  
SIMD compiler
23. **Kanishkan Vadivel**, ES 2017  
CGRA compiler
24. **Barry de Bruin**, ES, 2017  
Applicability of CNNs for Intel DSPs
25. **Arno Tiemersma**, ES, 2017  
*Constrained based code generation for CGRAs*
26. **Vishnu Pasupula**, ES, 2016  
*Scheduling and optimization of production printers*  
With Océ Venlo
27. **Sandeep Poddar**, ES, 2016  
*SKA Power Modelling*  
With ASTRON Dwingeloo
28. **Jos IJzerman**, ES, 2016  
*Vector support for Convolutional Neural Networks on Transport Triggered Architectures*  
With Tampere University of Technology, Finland
29. **Michael Adriaansen**, ES, 2016  
*LLVM based Compiler support for CGRAs (Coarse Grain Reconfigurable Arrays)*
30. **Mattia Fiumara**, EE, 2016  
*Convolutional Neural Networks on SIMD systems*
31. **Sander Vocke**, ES, 2016  
*Halide to C to SiliconHive / Intel Image Processing Unit*  
With Intel Eindhoven
32. **Jumana Mundichipparakkal**, ES, 2016  
*Fast binary simulation by binary translation*  
With Intel Eindhoven
33. **Bart van Dongen**, EE, 2016  
*Video distribution system*  
With Prodrive Eindhoven

34. **Stef van Son**, ES, 2016  
*OpenVX support for Intel processing platform*  
With Intel Eindhoven
35. **Stef Louwers**, ES, 2016  
*Multi-granularity arithmetic for CGRAs*
36. **Roel Oomen**, EE, 2016  
*Technology scaling prediction*  
With IMEC Eindhoven
37. **Ozgun Yalcinkaya**, ES, 2016  
*Video (TV) enhancement*  
With Sigma-Design, Waalre
38. **Gaurav Raina**, ES, 2016  
*Mapping Convolutional Neural Networks on a Heterogeneous Multi-Core*  
  
With RECORE, Enschede
39. **Thomas Sioutas**, ES, 2015  
*Many core DSP system mapping support*  
With Prodrive
40. **Peter Koek**, EE, 2015  
*DLP exploitation for SDF modelled applications*  
With NXP
41. **Matthias Schneider**, ES, 2015  
*Re-entry satellites: embedded system design*  
With DLR (Deutsches Zentrum für Luft- und Raumfahrt), Bremen
42. **Wishnu Pramadi**, ES, 2015  
*Automatic code generation for the ConvNet accelerator*
43. **Thieme Joziase**, ES, 2015  
*Face detection and tracking on GPU based system*  
  
With Altran, Eindhoven
44. **Bas Renet**, EE, 2015  
*Advanced debugging functionality for secure identification smart cards*  
With NXP, Eindhoven
45. **Grigoris Raptis**, EE, 2015  
*High-speed servo implementation on a hybrid (ARM/FPGA SoC) processing system*  
With ASML, Velthoven

46. **Han Lin**, ES, 2014  
*Low power memory system HW-SW co-design for wireless sensor node*  
With IMEC Eindhoven
47. **Miguel Emilio Oznaya Angeles**, Emb Systems, 2014  
*GPU-based real-time holography through time-domain signal processing*  
With Sorama, Eindhoven
48. **Petros Voudouris**, ES, 2014  
*Real-time GPU processing*
49. **Wouter Ouwens**, EE, 2014  
*Real-time contactless vibration detection with NAH in lithography systems using a GPU.*  
With Sorama, Eindhoven
50. **Shyam Balasubramanian**, ES, 2013  
*Store-and-Forward Networking Solutions with Autonomous Aerial Vehicles*  
With THALES, Huizen
51. **Koen Hausmans**, ES, 2013  
*Reducing Synchronization Overhead by Scaling Parallel Streaming Applications*  
With NXP
52. **Yannick van Bavel**, ES, 2013  
*Advanced ultrasound beam forming using GPGPU technology*  
With eSaote
53. **Ruizhou Xie**, ES, 2013  
*Flexible memory shuffling unit for a programmable neural processor*
54. **Rick Hilkens**, EE, 2013  
*Implementation and analysis of a real-time adaptation algorithm on an FPGA for steering a nonlinear interference suppressor*  
With EE-SPS
55. **Peter Broere**, ES, 2013  
*A memory-centric SIMD neural network accelerator: Balancing efficiency & flexibility*
56. **Martijn van den Dungen**, ES, 2013  
*Vision-based edge tracking for area optimization*  
With OTB, Eindhoven
57. **Luc Waeijen**, ES, 2013  
*Design Space Exploration of a Low-Energy Wide-SIMD*
58. **Hoisun Ng**, ES, 2013  
*Design and Evaluation of a Novel Programmable Accelerator for Digital Signal Processing*  
With IBM Zurich

59. **Luuk Mallens**, ES, 2013  
*A framework for data-access strategies in GPGPU programs*  
With VectorFabrics
60. **Sunil John**, ES, 2012  
*Parallel code generation for non-preemptively scheduled multiprocessor systems*  
With NXP
61. **Sohan Nandkumar Walimbe**, ES, 2012  
*Architectural leakage power minimization of scratchpad memories by application-driven subbanking*  
With IMEC-NL
62. **Pieter Custers**, EE, 2012  
*Algorithmic species: classifying program code for parallel computing*
63. **Roy van Doormaal**, ES, 2012  
*Parallel training of large scale neural networks: Performance Analysis & Prediction*
64. **Luuk Loeffen**, EE, 2012  
*Automated generation of IP Core wrapper for faster SoC integration using HLS*  
With NXP
65. **Twan Kamp**, EE, 2012  
*Dataflow-based Multi-ASIP Motion Control Platform on Chip*  
With ASML
66. **Johan Hendriks**, ES, 2012  
*High Level Synthesis: Performance Analysis and Code Optimization*
67. **Luke Lemmen**, ES, 2012  
*FPGA Firmware Qualification Framework; Using AXI Interconnect and Extended Debug Facilities*  
With Prodrive, Eindhoven
68. **Sheng Hao Wang**, EE, 2012  
*Saliency Detection on FPGA Using Accelerators and Evaluation of Algorithmic Skeletons*
69. **Rik Jongerius**, EE, 2012  
*Quantifying and Capturing the Semantics of Computational Problems in Contemporary Applications for Algorithmic Choice*  
With IBM research, Zurich
70. **Martien Spierings**, ES, 2011  
*Embedded platform selection based on the Roofline model; Applied to video content analysis*  
With Prodrive (together with Rob vd Voort)

71. **Rob van de Voort**, ES, 2011  
*Embedded platform selection based on the Roofline model; Applied to video content analysis*  
With Prodrive (together with Martien Spierings)
72. **Tim Vriends**, ES, 2011  
*Evaluation of High Level Synthesis for the implementation of Marker Detection on FPGA*
73. **Xuyuan Jin**, EE, 2011  
*Automatic Code Generation and Adaptive Grid Scheduling for GPU Cluster Computing*
74. **Levent Korkut**, ES, 2011  
*Hybrid Sensor Systems for Cost Efficient Egomotion Estimation*  
With Philips Research
75. **Shubhendu Sinha**, ES, 2011  
*Clustering Synchronous Dataflow Actors for finding Optimal Configuration of Configurable Hardware for Multiple Applications*  
With NXP
76. **Michiel Bosveld**, ES, 2011  
*Exploring the design space of a VLIW processor for LTE and LTE-A*  
With STEricsson
77. **Jarno van der Sanden**, ES, 2011  
*Evaluating the Performance and Portability of OpenCL*
78. **Wilco Belgraver Thisse**, EE, 2011  
*A comparative study of optical depth sensors for user interaction*  
With Philips Research
79. **Jingzhou Luo**, EE, 2011  
*A Low Cost Programmable LIW-SIMD Coprocessor for Filters and MAC-related Algorithms*  
With STEricsson
80. **Mark Wijtvliet**, ES, 2011  
*Design of a multi-electrode fish recognition system based on changing cross-sectional resistance*  
With Witteveen&Bos
81. **Kris Hoogendoorn**, EE, 2011  
*Inter-cluster Communication on Clustered SIMD Architectures*
82. **Martijn Koedam**, EE, 2011  
*Exploiting Inter and Intra Application Dynamism through System-Scenarios to Save Energy*
83. **Ronald van Gastel**, EE, 2011  
*Evaluation and mapping of hierarchical-temporal memory networks on an efficient platform*

84. **Tim van den Kerkhof**, EE, 2011  
*Real-time multi-scale TV image analysis on DSP, with application to image metrics, and control of image enhancement functions*  
With NXP
85. **Marc Brouns**, EE, 2010  
*Implementation of SIMD architecture on FPGA*
86. **Rick Boer**, ES, 2010  
*Interactive Free Viewpoint 3D TV Rendering Platform*  
With Silicon Hive
87. **Atilla Filiz**, ES, 2010  
*Analyzing the Feasibility of Real-Time Dense Stereo on a Dual DSP setup*
88. **Maurice Peemen**, EE, 2010  
*Mapping Convolutional Neural Networks on a Reconfigurable FPGA Platform*
89. **Qiao Peng**, EE, 2010  
*Design and Optimization of Digital Hearing Aid System Based on Silicon Hive Technology*  
With Silicon Hive
90. **Joost Hausmans**, ES, 2010  
*Resynchronization of Dataflow Graphs*  
With NXP
91. **Stefan Geuns**, ES, 2010  
*Parallelization of While-Loops in Nested Loop Programs for Real-time Multiprocessor Systems*  
With NXP
92. **Zhengjie Lu**, EE, 2010  
*MPSoC Platform Design and Simulation for Power Performance Estimation*  
With STEricsson
93. **Corne Kraaij**, EE, 2010  
*Exploring Loop Buffers for SIMD Architectures*
94. **Michiel Rooijackers**, EE, 2010  
*Design space exploration for scalable R-peak detection; Trading quality versus power*  
With Philips Research
95. **Wouter van der Put**, ES, 2010  
*Time-predictability of a computer system*  
With Prodrive



96. **Wouter van Heijningen**, EE  
*Testing mechatronic embedded control HW/SW using simulation and fault injection*  
With OCE
97. **Robert van Vooren**, EE, 2009  
*Observation for resource-constrained devices*
98. **Bart van Stiphout**, EE, 2009  
*Best view selection using multiple smart cameras*
99. **Gert-Jan van den Braak**, EE, 2009  
*Compile-time GPU Memory Access Optimizations*
100. **Xicai Chen**, EE, 2009  
*Design Space Exploration for Hough Transform Mapped to VLIW Architecture Exploring Subword Parallelism*  
With Silicon Hive
101. **Roel Jordans**, EE, 2009  
*Integration of observation into products: a case study with the Android platform*
102. **Jochem van der Meer**, EE, 2009  
*Analysis and design-space exploration of a dynamic interconnect for SIMD architectures*
103. **Cedric Nugteren**, ES, 2009  
*Improving CUDA's Compiler through the Visualization of Decoded GPU Binaries*
104. **She Dongrui**, ES, 2009  
*FPGA Platform for Emulation of Composable and Predictable MPSoC Power Management*
105. **Firew Siyoum**, ES, 2009  
*TLM-based Multi-core System Level Modeling and Simulation (TM2S)*  
With Recore
106. **Willisont Hayes**, ES, 2009  
*Memory Pattern Generation based on Specification and Environment*
107. **Zhenyu Ye**, ES, 2009  
*Architecture Exploration for Parallel Processing Systems*
108. **Julian Pallares Garcia**, Erasmus Valencia, 2009  
*POOSL on Transputers*  
Erasmus student
109. **Haibin Wang**, ES, 2009  
*Modeling and Performance Analysis for Light Control Subsystem*  
With ASML

110. **Frank Ophelders**, ES, 2009  
*A Tuneable Software Cache Coherence Protocol for Heterogeneous MPSoCs*  
With NXP
111. **Andrew Thomas Nelson**, ES, 2009  
*Conservative Application-Level Performance Analysis through Simulation of a Multiprocessor System on Chip*
112. **Rolf van de Burgt**, EE, 2008  
*Atalanta Wingman: Blimp positioning in a wireless sensor network*  
With DEVLAB
113. **Thom Gielen**, EE, 2008  
*Extracting SDF from sequential applications for MPSoC and implementation on FPGA*  
With NUS Singapore
114. **Alberto Falcon Garcia**, Erasmus Las Palmas, 2008  
Erasmus student
115. **Michael Koch**, EE, 2008  
*Distributed smart camera calibration using LED*  
With NXP
116. **Paul Meys**, EE, 2008  
*Mapping a YUV to RGB application onto Cell Broadband Engine and Nvidia Geforce 8*
117. **Onno Brunklaus**, EE, 2008  
*Implementing a scan-to-printer image chain on a massive parallel SIMD processor*  
With OCE
118. **Yifan He**, EE, 2008  
*Real-Time Hough Transform on 1-D SIMD Processors: Implementation and Architecture Exploration*  
With NXP
119. **Andre Boon**, EE, 2008  
*A Hybrid Processor Architecture for (Ir)regular Image Processing on an FPGA*  
With Prodrive
120. **Roy Phillipsen**, EE, 2008  
*PIR Model Driven Engineering*  
With ASML
121. **Bert van Moll**, EE, 2008  
*Fast and Accurate Protocol Specific Bus Modeling using TLM 2.0*  
With NXP

122. **Win King Wan**, ES, 2008  
*Evaluation and desing of multi-processor architectures*
123. **Tim Drijvers**, ES, 2008  
*Fast Huffman Decoding by Exploiting Data level Parallelism*  
With Silicon Hive
124. **Abhiram Ganesh**, Exchange student Munipal, India, 2008  
*Gesture analysis and mapping to Xetal like platforms*
125. **Raymond Frijns**, 2008  
*DC-SIMD : Dynamic Communication for SIMD processors*
126. **Daan Alberga**, 2008  
*An implementation of Reactive Process Networks*
127. **Rogier Thus**, 2007  
*Generation of Models Based on Modelling Patterns*
128. **Mark Slegers**, 2007  
*Prototyping of Dynamic Reconfiguration in a NoC based System on Chip*  
With Silicon Hive
129. **Tijs Versteegde**, 2007  
*Development of Sesia: a VLIW Processor for Multi-Standard Turbo Decoding*  
With Silicon Hive
130. **Teresa Median**, Erasmus, Las Palmas, 2006  
*Fast modelling and analysis of NoC-based MPSoCs*  
Erasmus student
131. **Dai Rui**, TU/e-NUS joined master, 2005  
*Real time clustering and visualization of dynamic information using a massively parallel embedded processor*  
With OCE
132. **Michiel Oostindie**, EE, 2005  
*Exploring boundaries in game processing*
133. **Veena Parashuram**, EE, 2005  
*Mapping object detection onto a heterogeneous multiprocessor vision platform*  
With Philips
134. **Isabel Marquez**, Erasmus, Las Palmas, 2005  
*Hardware Communication Services for Synchronous Data Flow in the Mini-NoC*  
Erasmus student

135. **Jose C. Prats Ortiz**, Erasmus, Las Palmas, 2005  
*Design of components for a NoC-based MPSoC Platform; Adding a shared memory node to the mNoC*  
Erasmus student
136. **Jos Hulzink**, EE, 2004  
*Optimization of Ultra Long Instruction Word processors for the Software Defined Radio (SDR) domain*  
With Silicon Hive
137. **Tycho van Meeuwen**, EE, 2002  
*Data-cache conflict-miss reduction by high-level data-layout transformations*  
With IMEC Leuven

### ***Master students supervised at TUDelft***

Period: Febr 1986-August 2001

1. **Anne Bezemer**  
Modeling and Design Space Exploration of Low Power TTAs (Transport Triggered Architectures)  
Finished: September 2003
2. **Jari Heikkinen**  
Hardware support for geometric spectral transforms  
Student of Prof Jarmo Takala, Tampere University of Technology, Finland
3. **Jos Nelissen**  
Real-time image stabilization and noise reduction using TTAs
4. **Sebastiaan de Smet**  
Real-time image stabilization and noise reduction using TTAs
5. **Ivo Jansen**  
Advanced Scheduling for TTAs
6. **Stephan Lichtendahl**  
A TTA based processor for JVM (Java Virtual Machine) code  
1999
7. **Arwin Smit**  
MOVE Processor Generator  
2000

8. **Guido Tjia**  
TTA exception support  
2000
9. **I-Chih Kang**  
March 1999  
Topic: Virtual time latching Load-store unit for TTAs
10. **Alexander Lint**  
Februari 1999  
Topic: A real-time pipe organ synthesizer with integrated effects
11. **Maarten Boekhold**, September 1998  
Title: A Programamble Code Transformation Engine
12. **Robert J. de Gruijl**, September 1998  
Title: Design of a digital pipe organ; a flexible approach  
Thesis work at Eminent, digital organ company at Lelystad, The Netherlands
13. **Arjen M. van der Weijden**, August 1998  
Title: Design and Implementation of the MOCCA Processor
14. **Henk Punt**, August 1998  
Title: Microcode compaction for Mistral 2 processor and its implementation in the I.McIC
15. **Henjo Schot**, July 1998  
Title: Design of an application specific processor for high performance image processing
16. **Steven Roos**, July 1997  
Title: Design and implementation of an advanced instruction fetch unit for the MOVE framework.  
Continued as PhD student on the ReMOVE architecture
17. **A.H. (Noud) van Klinken**, September 1997  
Title: Preprocesssing signals for digital television
18. **Niels Carpentier**  
Advanced speculative load-store support within a superscalar architecture
19. **Andrea Cilio**, July 1996  
Title: Comparative analysis between automatic design methodology and manual of an embedded system for MPEG Audio decoding  
Student of Alessandro De Gloria, DIBE, University of Genua, Italy
20. **Dennis N. Moolenaar**, May 1996  
Title: System specification and storage architecture exploration for two video compression standards

21. **Erwin C. Abrahamse**, September 1996  
Title: Determining Execution Frequencies of Instructions without Profiling: A Survey
22. **Theo Baan**, 1996  
Title: Design and Implementation of a Load-Store Unit for MOVE
23. **Bas K. van Houte**, January 1996  
Title: MOVE-design, Design and Implementation of a Graphical User Interface for the MOVE-framework
24. **Marcel van der Lem**, 1995  
Title: Implementation of realtime video compression, conform the MPEG standard, using a Transport Triggered Architecture.
25. **Jeroen Hordijk**, February 1995  
Title: Exploiting the Instruction-level Parallelism of the Software TV applications using the MOVE Processor Framework  
Continued as PhD student
26. **Lourens J. Visser**, August 1995  
Title: Survey and Comparison of Methods for Design for Testability, a MOVE3INT Case study
27. **Marnix Arnold**, June 1995  
Title: Synthesis and characterization of MOVE configurations, a new processor generator and a modeler proposal  
Continued as PhD student in the MOVE project
28. **Marcel R. van der Laan**, June 1995  
Title: MOVEmate: A Multifunctional Area and Timing Estimator for the MOVE framework
29. **Tobias J. Nijweide**, March 1994  
Title: Implementing DESP for MOVE
30. **Wilco N. van Hoogstraeten**, July 1994  
Title: Optimistic Distributed VHDL Simulation
31. **Reinoud Lamberts**, January 1994  
Title: A MOVE Processor Generator
32. **Frans van Camp**, August 1993  
Title: Real-time motion estimation within the MOVE framework
33. **Maarten Hofman**, May 1993  
Title: Design and modeling of MOVE processors using VHDL and COMPASS
34. **Andre van der Avoird**, September 1993  
Title: Automatic generation of pipelined multipliers

35. **Arno F. Roelofs**, August 1993  
Title: Force Directed Scheduling for Transport Triggered Architectures
36. **Guillermo Cuppers**, May 1993  
Title: Design and Implementation of a Load/Store Unit for the MOVE31INT Processor.
37. **Huib T. Van Grol**, December 1992  
Title: Performance Measurement at Generation-Based Garbage Collectors
38. **Harry E. Snier**, December 1992  
Title: A systematic view on binary adders
39. **Rene Bodestaff**, December 1992  
Title: Fast computing on Silicon
40. **Jan Hoogerbrugge**, December 1991  
Title: Software Pipelining for Transport-Triggered Architectures  
Continued as PhD student in the MOVE project
41. **Rogier E. Wolf**, December 1991  
Design and implementation of a communication processor
42. **J.G.E. (Eddy) Olk**, August 1991  
Title: Communication Processor for massive parallel MIMD Systems  
Continued as TWAIO (2-years post-graduate program) on PARSE, parallel architecture simulator environment
43. **Theo P. Borst**, June 1989  
Title: Unification Parallelism in Prolog
44. **Paul E. Schuurmans**, September 1989  
Title: Performance Analysis of Two-semispace Garbage Collectors
45. **Ignatio G. Alves**, March 1989  
Title: Explicit Concurrency in Logic Languages
46. **Hans J. van Gelderen**, July 1989  
Title: Tela-Time Garbage Collection in Heap-oriented Computer Systems
47. **Tom Veldman**, August 1989  
Title: Garbage Collection in Area-based Storage Systems
48. **A.C.J. Beekman**, September 1988  
Title: Highly Parallel Dataflow and Logic Architectures: Main Principles and Design Considerations
49. **F.P.E. van Ris**, August 1988  
Title: Accelerating shading algorithms by using parallel processors

50. **P.J. Brand**, February 1988  
Title: Verification and Test in the SINEC-SV System
51. **R.E. Jacobs**, March 1988  
Title: Parallelism in PostScript
52. **Gerard J. Brouwer**, August 1988  
Title: Code Generation
53. **J.J. Lous**, August 1988  
Title: Performance Improvement Analysis for Graphical Workstations
54. **Qi Cui**, August, 1988  
Title: Research on optimizing compilers
55. **Frank W. ten Wolde**, September 1988  
Title: Lisp and its implementation
56. **Marcel Mol**, September 1988  
Title: Lisp and its implementation
57. **Hans Kinwel**, November 1987  
Title: Prolog Implementations and Prolog Machines
58. **C. Tjahjadi**, December 1987  
Title: \*IT\* Scheme abstract machine
59. **Marek J. Druzdzel**, February 1987  
Title: Current Trends in Computer Architecture and their Relation to the LISP Programming Language
60. **Gerard J. van Bochoven**, February 1987  
Title: Garbage collection in heap oriented computer systems
61. **Arjan Koster**, June 1987  
Title: Between SPICE LISP and Machine
62. **Paul A.W. van Niekerk**, November 1986  
Title: Control Flow LISP Machines
63. **Paul N. Ruizendaal**, July 1986  
Title: On the Run-Time Model of the LISP Language
64. **Wim Koelewijn jr.**, July 1986  
Title: On the Run-Time Model of the LISP Language



