Automatic Generation of Flexible Parallel Port in 3D-SICs

➢ Project Description

Testing is an essential step after the fabrication of integrated circuits (ICs, chips) to guarantee that only good chips are delivered to customers. In order to perform testing of chips, dedicated hardware has to be inserted during the design phase of ICs.

Three-dimensional stacked integrated circuits (3D-SICs) are the next-generation ICs to enable the further scaling of semiconductor technology. Similar to two-dimensional (2D) chips, the insertion of test infrastructure into 3D-SICs is essential. In the context of IEEE Std P1838, a standard-under-development for test infrastructure for 3D-SICs, a flexible parallel port (FPP) has been developed. Furthermore, a description language has been proposed by imec to describe the formation of the FPP in any particular 3D-SIC. The aim of this project is to develop an automatic design flow to generate an FPP based on the description language and to integrate the generated FPP into a 3D-SIC.

➢ What you are expected to do

In this project, you are expected to develop the automatic flow that is described in the section above for the electronic design automation (EDA) tools of Cadence. You need to find out / develop a parser to parse the FPP description language. Afterwards, you need to use scripts to translate the information that you get from the FPP description language to hardware testing structures that are compatible to Cadence tools. The whole flow will be integrated as a single deliverable.

➢ What you get

1. Two supervisors: Dr. Hailong Jiao, Electronic Systems group, Department of Electrical Engineering, TU/e
   Mr. Erik Jan Marinissen, Principal Scientist, imec, Leuven, Belgium (IEEE Fellow)
   You will have the access to both academic and industrial design and test experience.
2. Access to a variety of state-of-the-art EDA tools from Cadence.
3. Possibility to do the project at imec, Leuven, Belgium, if you prefer.
3. Very good chance to publish a couple of IEEE conference/journal papers.

➢ Project duration

Master final project (six to nine months).

➢ Contact

If you are interested, please send an email to Dr. Hailong Jiao (h.jiao@tue.nl). You can find more information on the webpage http://www.es.ele.tue.nl/~hjiao/.