Synchronous Latency Insensitive Design in Æthereal NoC

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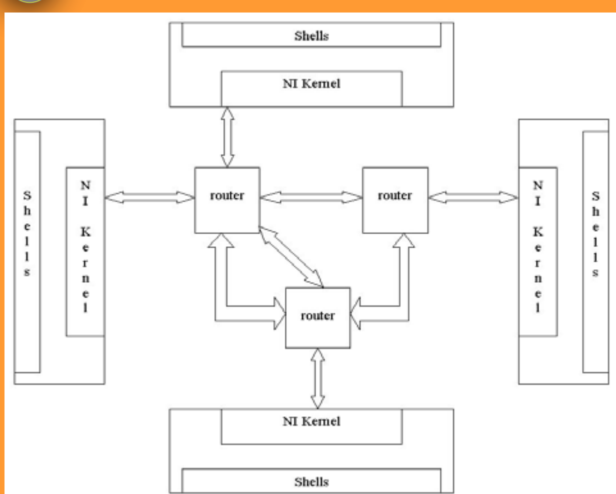
Abstract

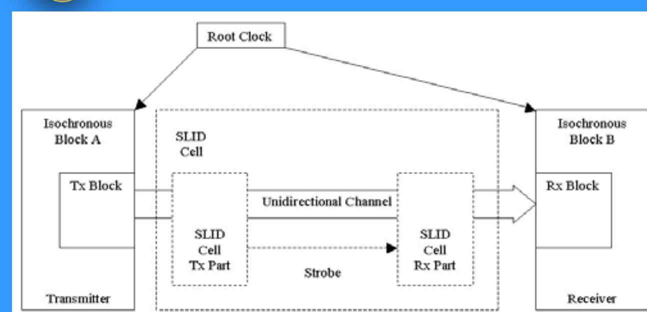
In this paper the Synchronous Latency Insensitive Design [1] (SLID) method to mitigate timing problems due to global wire delays in Æthereal NoC is proposed. This method follows closely a fully synchronous design flow and utilizes only true digital library elements, which does not change the original design flow and libraries of Æthereal. A few clock cycles latency is inserted to every connection between different functional units. This latency is used to automatically absorb unknown global interconnect delays, unknown global clock skews and other timing uncertainties. The introduced SLID method may substantially cut down the timing closure effort in Æthereal NoC system design, and other large scale, high frequency digital designs carried out in Deep Sub-Micron (DSM) technologies.

An Æthereal NoC as a Design Example



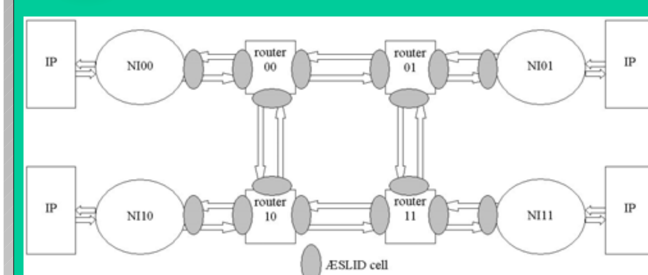
Æthereal [2] Network on Chip (NoC) (see figure above) is an advanced intercommunication solution to large scale System on Chip (SoC). It plays a central role in integrating IPs with diverse communication requirements. Æthereal and other NoCs usually have long interconnects in their design. A general disadvantage of long interconnects is that they introduce uncertainties like transmission delay over buses or global clock skews. It has been recognized that integrated circuits in DSM technologies exhibit increased timing problems due to increased clock frequencies, increased complexity and increased wire delays. These problems manifest themselves as a severe increase in verification cost (timing closure), increased problems to scale up the clock frequency and increased effort for clock distribution.

The SLID Scheme



This paper proposes the SLID scheme to ease the timing problems in Æthereal NoC. The main goal is to keep its fully synchronous design flow even for large high-speed designs in DSM processes. The idea is to manage the inevitable wire delays already at architecture level, and then guarantee that the functional description at this level is valid all the way to layout.

SLID Scheme Implemented in a 2*2 Æthereal NoC



The implementation of the SLID scheme (see figure above) in Æthereal is based on the partition of a large design into isochronous blocks (e.g. routers, NIs), still keeping global synchronism. Each router/NI should be small enough not to exhibit severe wire delays. Between the routers and NIs an extra delay (pipelining) is inserted. This extra delay is later applied to automatically mitigate unknown wire delays and clock skews. Thus the proposed SLID scheme simplifies timing closure and relaxes clock distribution constraints of Æthereal NoC.

[1] A. Edman and C. Svensson, "Timing Closure through a Globally Synchronous, Timing Partitioned Design Methodology", Proc 41st Design Automation Conference, pp. 71-74, June 2004
[2] John Dielissen, Andrei Rădulescu, Kees Goossens and Edwin Rijpkema, "Concepts and Implementation of the Philips Network-on-Chip". IP-Based SOC Design, Grenoble, November 2003