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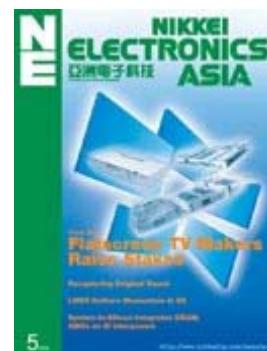
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Columns

## Design View from Japan: ST, Philips Steal Show at DATE 06

Design, Automation & Test in Europe 2006 (DATE 06), covering integrated circuit (IC) design and test, was held from March 6 to 10 in Munich, Germany. Visitors to the show this year were especially interested in announcements from European system-on-chip (SoC) manufacturer Royal Philips Electronics NV of the Netherlands, and Italian-French joint venture ST Microelectronics NV (ST).

ST and Philips announced the use of an intellectual property (IP) interface standard called SPIRIT (Structure for Packaging, Integrating and Re-using IP within Tool-flows) in a SoC. SPIRIT was developed by firms including ST Microelectronics, Philips, and ARM Ltd of the UK to facilitate verification of SoCs with multiple IP cores. If both the IP core and the electronic design automation (EDA) tools used for verification comply with the SPIRIT standard, it is much simpler to construct a verification environment.



**DATE Keynote Speech** Rene Penning de Vries, senior VP & CTO, Philips Semiconductors. (Photo by Nikkei Microdevices)

SPIRIT is an IP core standard and therefore often viewed as the European version of the Virtual Socket Interface Alliance (VSIA) of the US, but the objective is different. The VSIA is primarily aimed at improving efficiency in physical design, while SPIRIT instead aims at improving verification efficiency at the register transfer level (RTL) and upstream. While the VSIA was unable to achieve its initial objective and changed course in midstream, SPIRIT appears to

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have been making steady progress. It acquired a Project Authorization Request (PAR) number from the Institute of Electrical and Electronics Engineers Inc (IEEE) of the US in August 2005, and is thought to be just about ready to become an IEEE standard.

### SPIRIT, 65nm SoCs

Philips and ST also announced the use of the SPIRIT standard in the development of SoCs using 65nm nodes, which is a state-of-the-art process technology, at DATE 06. ST, for example, disclosed that it is using the SPIRIT standard to verify the STB7200 multimedia processor SoC, now in development for the next generation of set-top boxes. The firm developed its own tool to automatically generate SPIRIT data (metadata) required to integrate the IP core, and used the same tool on the IP core in the announced SoC. The IP cores were integrated using the coreAssembler EDA tool from Synopsys Inc of the US. The STB7200 was the first application in a development project by ST, but it is also being used in the development of a SoC for mobile phones.

Philips, meanwhile, presented an application of its Nx-Builder SoC development system based on SPIRIT. Two examples were discussed. The first chip was a SoC for automotive communication designed to the FlexRay standard. The firm issued a press release on the chip in October 2005. The second application was a SoC platform using 65nm node process technology, announced in early March 2006. The platform is intended for use with consumer electronics SoCs, and stresses low dissipation. The processor core is an ARM1176JZF-S.

### Investigating NoCs

In addition to the SPIRIT announcement, Philips Research Laboratories also presented the results of an investigation into the utility of using network-on-chip (NoC) technology to interconnect multiple ICs. NoC technology is viewed as a replacement to the on-chip bus, and offers advantages such as the ability to interconnect multiple IP cores, and increased data freedom in handling data between IP cores. Compared to a bus, however, it also suffers penalties in terms of chip area and dissipation.

Philips Research Labs redesigned an existing bus-type application-specific IC (ASIC) for TVs to use NoC technology, and evaluated the resulting disadvantages. The change from bus to NoC increased chip area by 4.4%, and the 300MHz operating frequency of the NoC region increased dissipation by 10.8%. When the network configuration was changed from 2x2 to 1x3, however, the operating frequency of the NoC region dropped to 160MHz, with an increase in dissipation of only 5.4%.

The 1x3 configuration does reduce the degree of network freedom, however.

According to Kees Goossens of Philips Research Labs, the investigation indicated that the penalty is sufficiently low. As a result, designer interest in NoCs is rising, and he commented that the development of the first SoCs using NoC technology would be started in 2007.

by *Ikutaro Kojima*

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