Introduction

Recent developments in modern embedded system technology have enabled the development of complex heterogeneous multiprocessor systems on single chips (MPSoCs) and created an upsurge in high-performance and low-power embedded system design. My research focuses on the automatic instruction-set synthesis and application mapping for customizable VLIW-based ASIPs.

Strategy

Instruction-set synthesis is performed at different levels of granularity according to the available exploration time and design demands. The mapping of various buffers to different memories and possible vectorization are not considered and must be provided by higher level exploration.

A general framework (shown below) is constructed to provide four levels (shown to the right) of exploration granularity, depending on the components considered from the library.

Instruction-set synthesis in steps

1. Bounds on instruction-level parallelism
2. Basic instruction-set synthesis (simple operations)
3. Advanced instruction-set synthesis (operation patterns)
4. Full instruction-set synthesis (custom operations)

Experimental results

The first experimental results on instruction-level parallelism estimation have been published [1] and improved results are available. Demonstrating that the number of issue-slots can be determined quite efficiently. Allowing for early feedback on possible designs.

Work progress

1. Parallelism estimation:
   – Both CP and heuristic versions available
   – Verification in progress

2. Basic instruction-set synthesis
   – 80% (CP version), 10% (heuristic version)

3. Advanced instruction-set synthesis
   – 0% (depends on basic instruction-set synthesis)

4. Full instruction-set synthesis
   – 0% (result of advanced ISS + custom FU creation)

References


ASIP micro-architecture synthesis
ASAM Project
Roel Jordans
Department of Electrical Engineering / Electronic Systems

Project description

Automatic Architecture Synthesis and Application Mapping (ASAM)

ASAM is a research project in the framework of the European ARTEMIS Research Program and ARTEMIS Joint Undertaking - the public-private partnership for R&D in Embedded Systems.

ASAM targets a uniform process of automatic architecture synthesis and application mapping for heterogeneous multi-processor embedded systems based on adaptable and extendable ASIPs. It aims to define a new unified design methodology, as well as, related automated synthesis and prototyping tool-chains. The new design environment will allow rapid exploration of the high-level algorithm and architecture design spaces, as well as, an efficient automation of the final system synthesis, and in consequence, quick development of high-quality designs.

Within the context of the ASAM project, Roel Jordans will be working on the micro-architecture design space exploration of single ASIP/application-part pairs. His task focuses on the exploration of the data-path organization and instruction-set synthesis of the ASIP: Automatically determining the number of issue slots, the instruction-set for each issue slot, and the required sizes for the register files based on the target application, a high level memory mapping, and a given set of optimization criteria.

Biography

Roel Jordans is a PhD student in the Electronic Systems group at the Department of Electrical Engineering at Eindhoven University of Technology. His research areas include ASIP micro-architecture synthesis, instruction set synthesis, and application modeling. He has received his Masters in Electrical Engineering from Eindhoven University of Technology (Eindhoven, NL) and Bachelors from Fontys University of Applied Sciences (Eindhoven, NL).