Recent developments in modern embedded system technology have enabled the development of complex heterogeneous multiprocessor systems on single chips (MPSoCs) and created an up surge in high-performance and low-power embedded system design. This poster focuses on the automatic architecture synthesis, application restructuring and mapping for customizable ASIP-based MPSoCs [1].

Application specific processors deliver high performance comparable to hardwired ASICs while providing the flexibility of programmable processors. However, their various parameters to explore result in a difficult DSE problem.

Example parameters include:
- Local memory hierarchy
- Local communication structure
- Number and size of register files
- Number and kind of issue-slots
- Instruction-set of each issue slot
- Application specific instructions
- Parallel execution structures
- Application restructuring to efficiently exploit the parallel structures

FPGA based prototyping provides a fast and accurate performance feedback for a refined DSE.