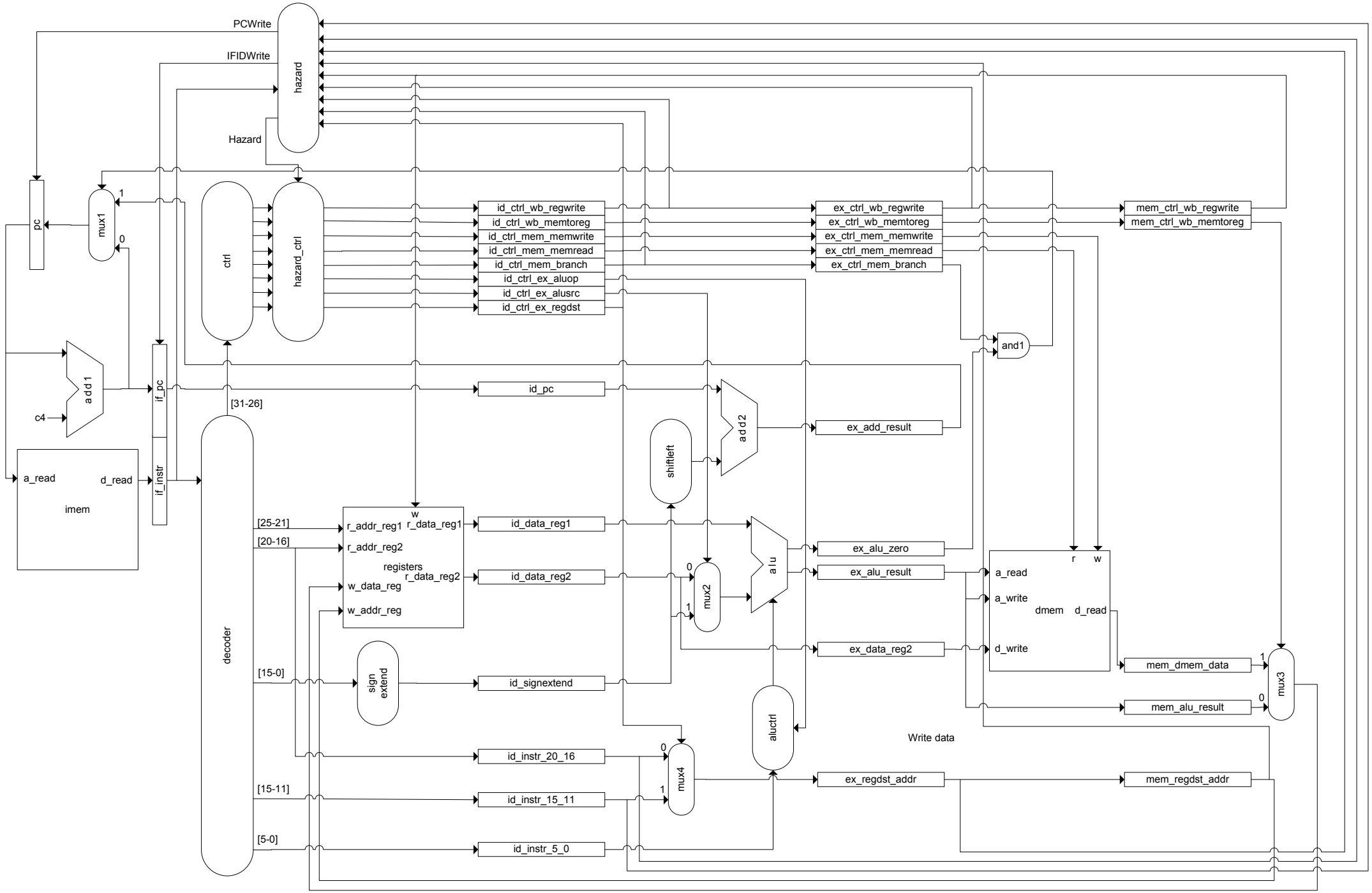
PCWrite
IFIDWrite
hazard
Hazard
pc
mux1
1
0
ctrl
hazard_ctrl
id_ctrl_wb_regwrite
id_ctrl_wb_memtoreg
id_ctrl_mem_memwrite
id_ctrl_mem_memread
id_ctrl_mem_branch
id_ctrl_ex_aluop
id_ctrl_ex_alusrc
id_ctrl_ex_regdst
ex_ctrl_wb_regwrite
ex_ctrl_wb_memtoreg
ex_ctrl_mem_memwrite
ex_ctrl_mem_memread
ex_ctrl_mem_branch
mem_ctrl_wb_regwrite
mem_ctrl_wb_memtoreg
and1
add1
c4
if_pc
if_instr
id_pc
[31-26]
add2
ex_add_result
shiftleft
a_read
d_read
imem
[25-21]
[20-16]
w
r_addr_reg1
r_data_reg1
r_addr_reg2
registers
r_data_reg2
w_data_reg
w_addr_reg
id_data_reg1
id_data_reg2
ex_alu_zero
ex_alu_result
alu
mux2
0
1
r
w
a_read
a_write
dmem
d_read
d_write
ex_data_reg2
decoder
[15-0]
sign extend
id_signextend
mem_dmem_data
mem_alu_result
mux3
aluctrl
Write data
id_instr_20_16
mux4
[15-11]
id_instr_15_11
ex_regdst_addr
mem_regdst_addr
[5-0]
id_instr_5_0