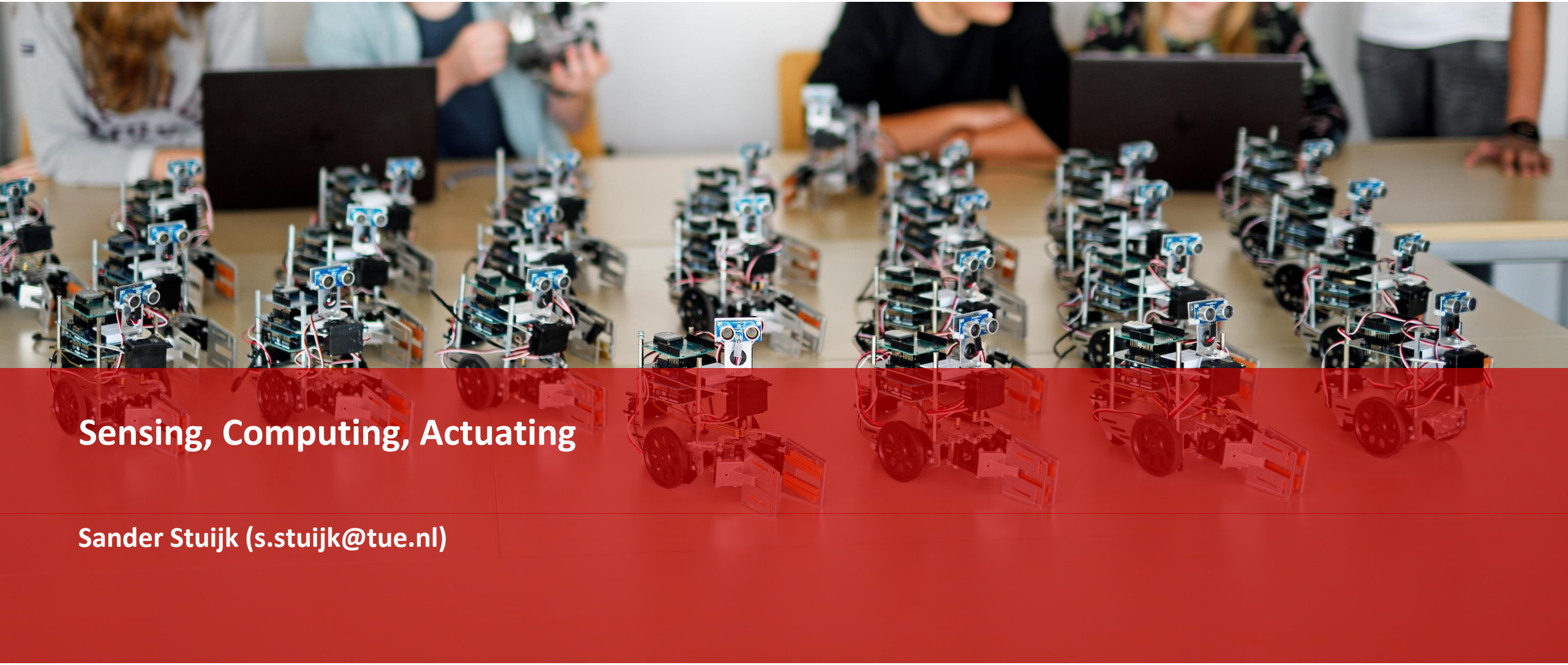


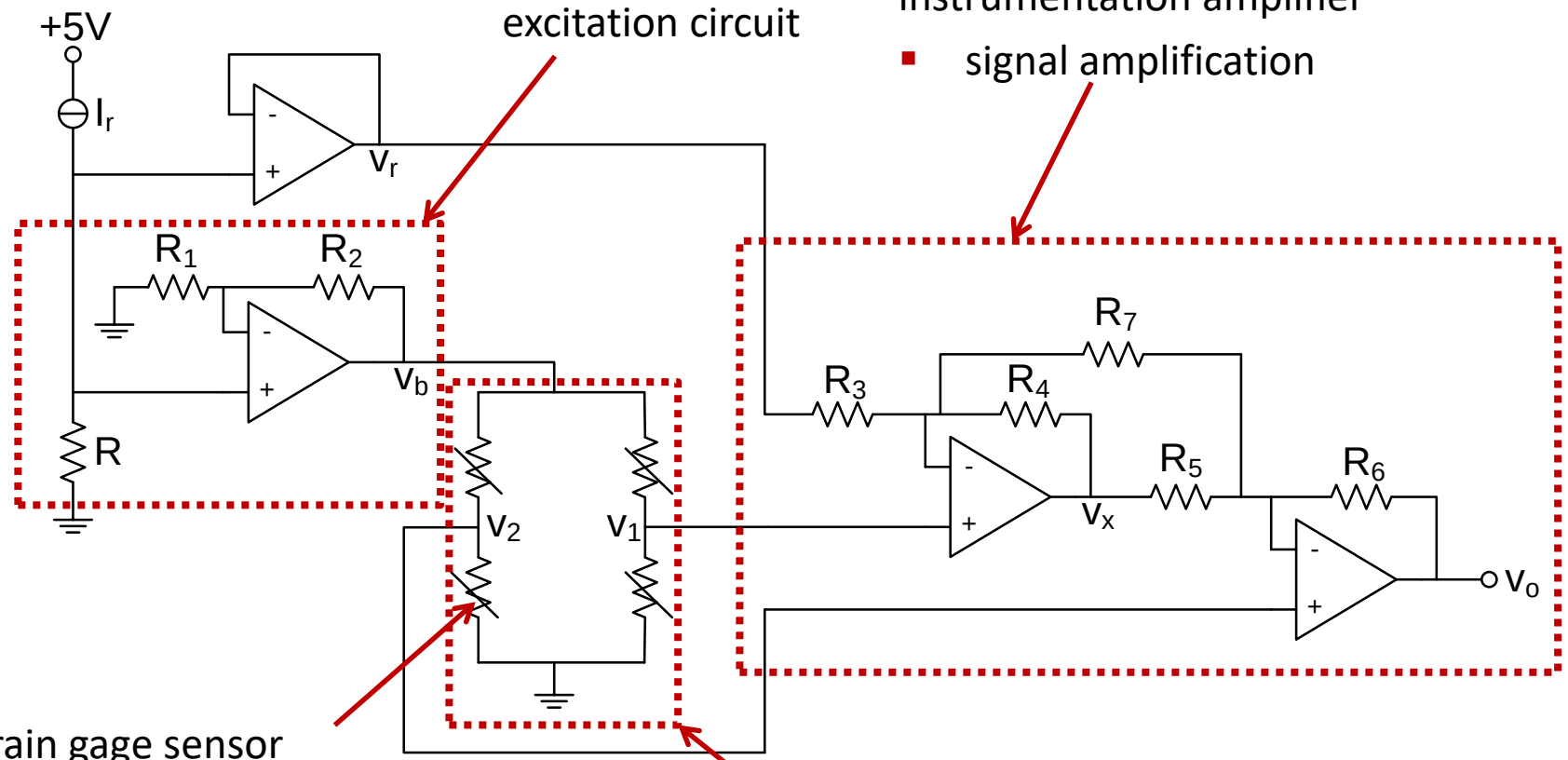
# Sensing, Computing, Actuating

Sander Stuijk (s.stuijk@tue.nl)

# ANALOG-DIGITAL CONVERSION

(Chapter 2.7)

# Example – pressure sensor




excitation circuit

instrumentation amplifier

- signal amplification

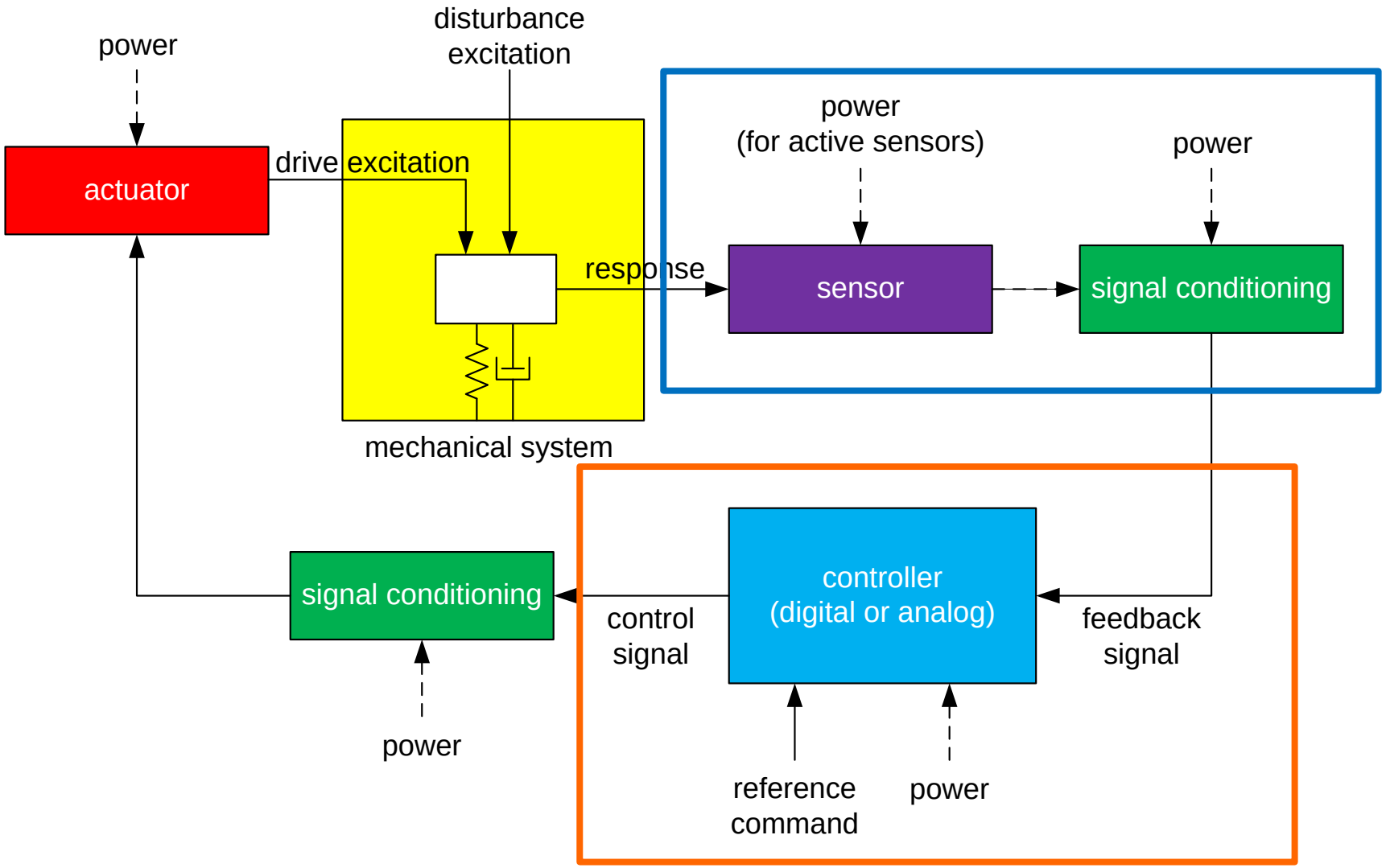
strain gage sensor

- active sensor
- absolute sensor
- contact sensor

signal processing circuit

- bridge circuit
- remove error sources (e.g. temperature)
- remove offset voltage
- improve linearity
- improve sensitivity

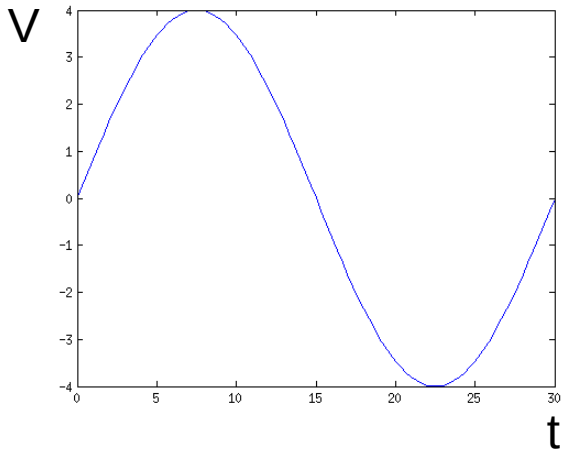
# Control system



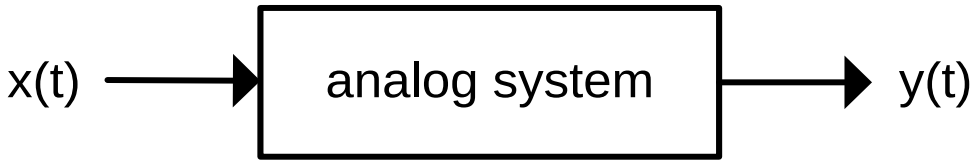
# Analog signals and systems

- most physical signals are continuous
  - speech and music signals, biomedical signals
  - most communication signals that are broadcast through the air

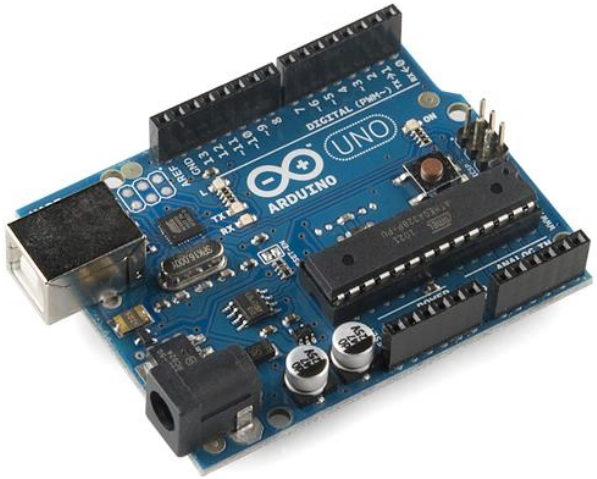
- analog signal
  - continuous in time
  - continuous in value (amplitude)




- analog system
  - works directly on analog signals
  - circuits: resistors, capacitors, transistors, op-amps, …



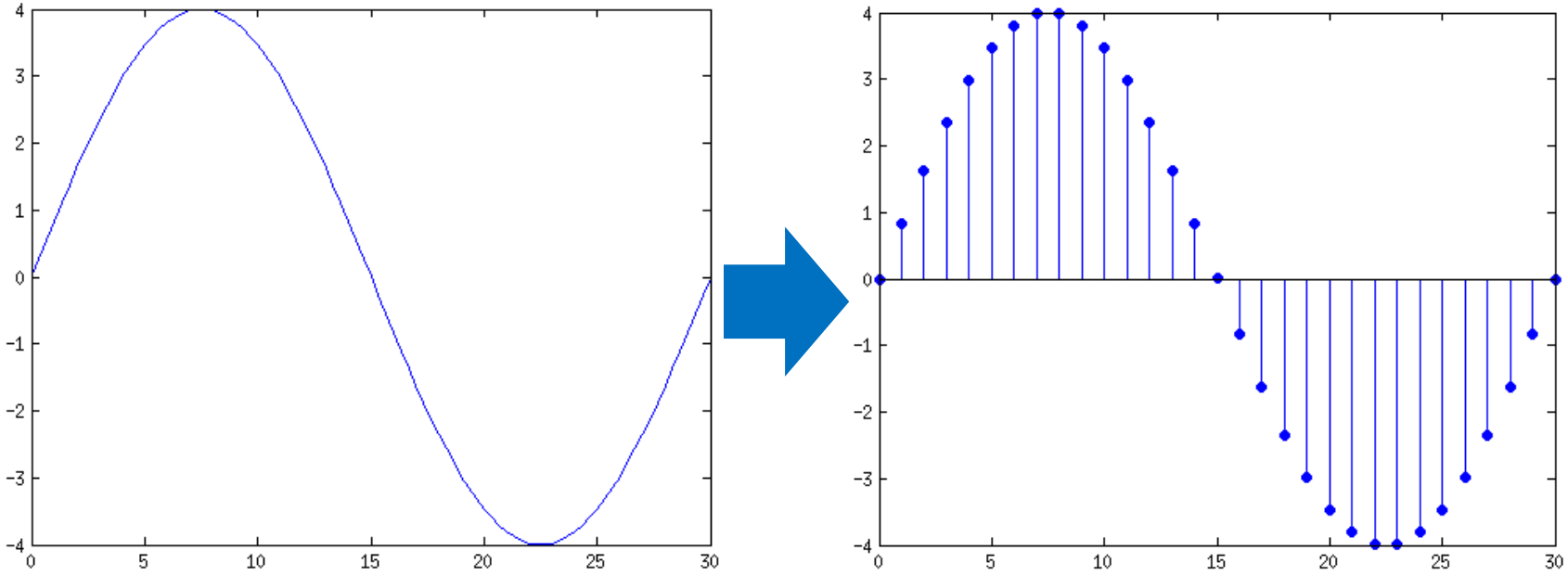
# Digital systems




- digital systems
  - computers, microprocessors, embedded processors, micro controllers, …
- digital signal
  - discrete in time
  - discrete in value
- advantages of digital systems compared to analog systems
  - it is easier to process signals
  - it is easier to store signals
  - it is easier to transmit signals

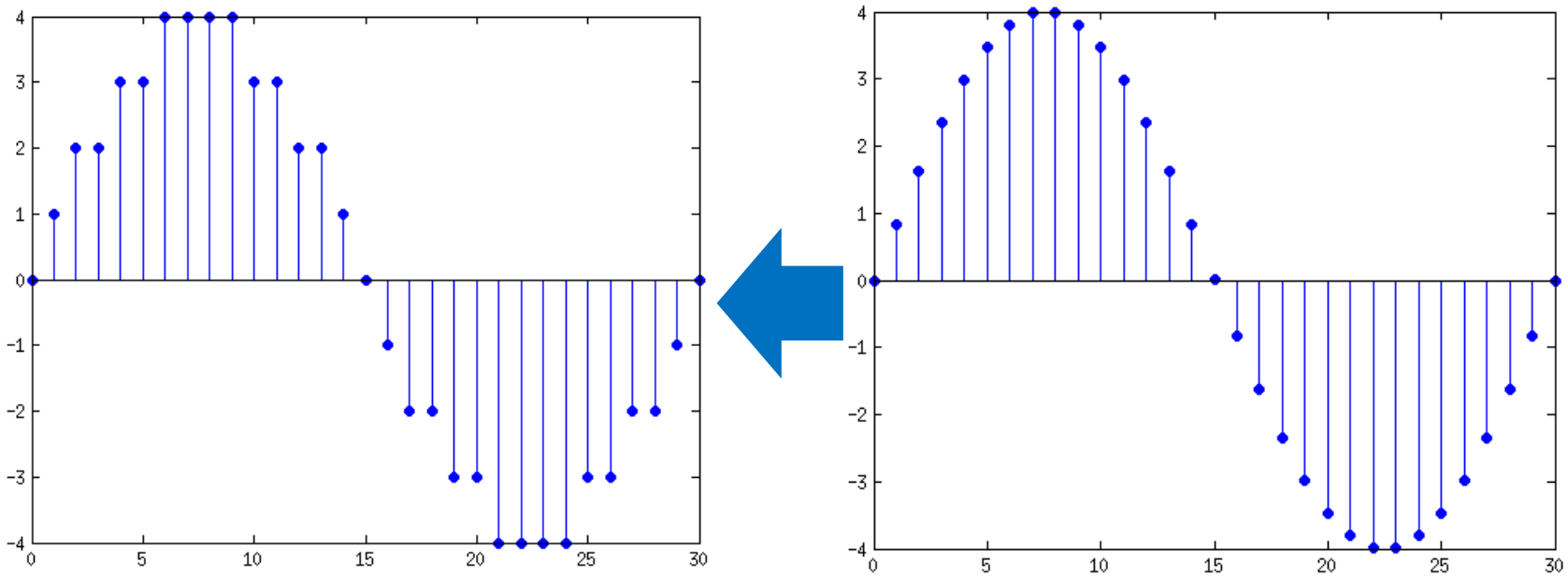
# Conversion to digital form

- limitations of digital systems
  - cannot deal with continuous-time signals
    - solution: sample signal at regular time interval



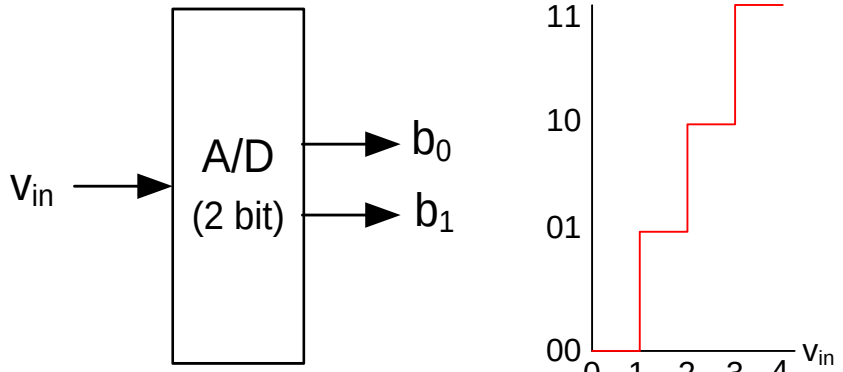
# Conversion to digital form

- limitations of digital systems
  - cannot deal with continuous-time signals
    - solution: sample signal at regular time interval
  - cannot store values with a continuous range
    - solution: approximate continuous value with digital value

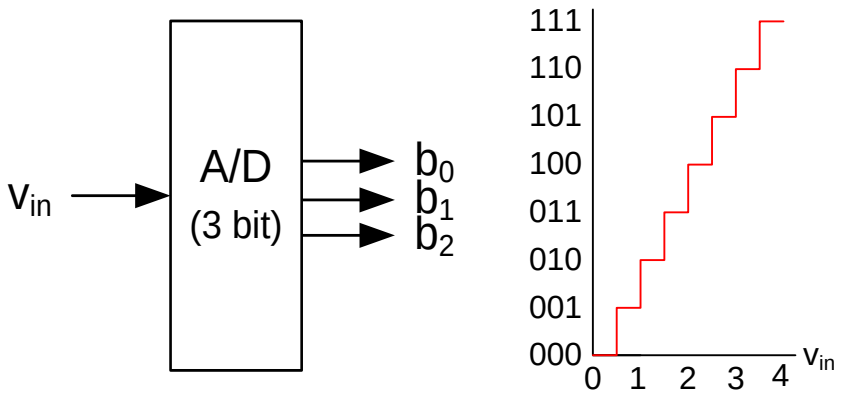


# Conversion to digital form

- analog signal digitized using ADC
- ADC determines resolution of sensor system
- resolution is smallest change in input which can be sensed
- 2-bit A/D converter (assume max input voltage = 4V)
  - $2^2$ = 4 levels
  - resolution: 1V/bit




- 3-bit A/D converter
  - $2^3$ = 8 levels
  - resolution: 0.5V/bit



# Conversion to digital form

- analog signal digitized using ADC
- ADC determines resolution of sensor system
- resolution is smallest change in input which can be sensed
- **how many bits should an A/D converter have to achieve a resolution of 3.5mV/bit if its maximal input voltage is 4V?**
- in general it holds that

$$n = \left\lceil \frac{\log\left(\frac{V_{\max}}{resolution\ V/bit}\right)}{\log(2)} \right\rceil$$

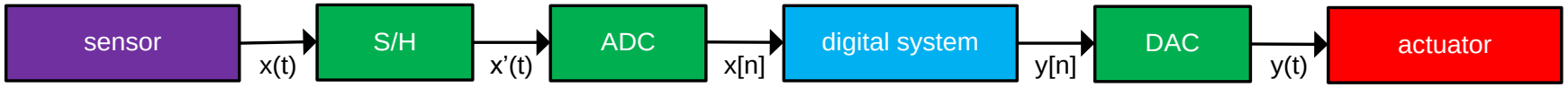
- substituting values gives

$$n = \left\lceil \frac{\log\left(\frac{4V}{3.5 \cdot 10^{-3} V/bit}\right)}{\log(2)} \right\rceil = 11bit$$

# Analog signals and digital systems

- digital system works on digitized samples of the signal


- connecting the analog and digital world




  - S/H – sample and hold circuit
  - ADC – analog to digital conversion
  - DAC – digital to analog conversion

# Weighted-resistor DAC

- **what is the output voltage Vo of the weighted-resistor DAC in terms of the input bits (digital data – $b_i$)?**
- Kirchhoff current law at node A
  - use VA = 0 V

$$\frac{v_{n-1}}{R}+\frac{v_{n-2}}{2R}+\ldots+\frac{v_0}{2^{n-1}R}+\frac{v_o}{R/2}=0$$

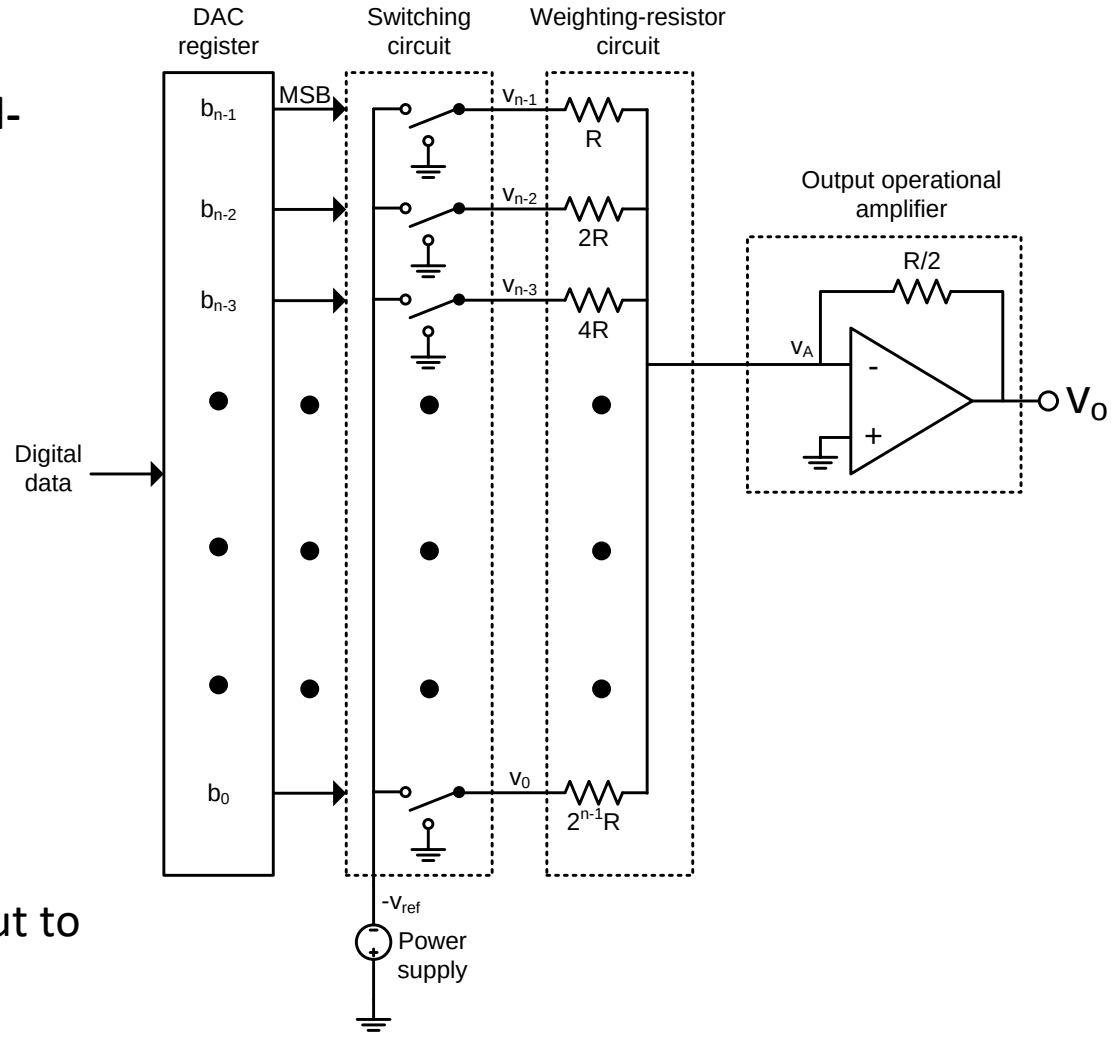
- relation voltage $v_i$ and bit $b_i$

$$v_i=-b_i\cdot v_{ref}$$

- output voltage

$$v_o=\left(b_{n-1}+\frac{b_{n-2}}{2}+\ldots+\frac{b_0}{2^{n-1}}\right)\frac{v_{ref}}{2}$$

- output voltage proportional to digital data input to DAC



# Weighted-resistor DAC

- **what is the output voltage Vo of the weighted-resistor DAC when all bits are equal to 1?**
- output voltage

$$v_o = \left( b_{n-1} + \frac{b_{n-2}}{2} + \ldots + \frac{b_0}{2^{n-1}} \right) \frac{v_{ref}}{2}$$

- full-scale voltage (all $b_i = 1$)

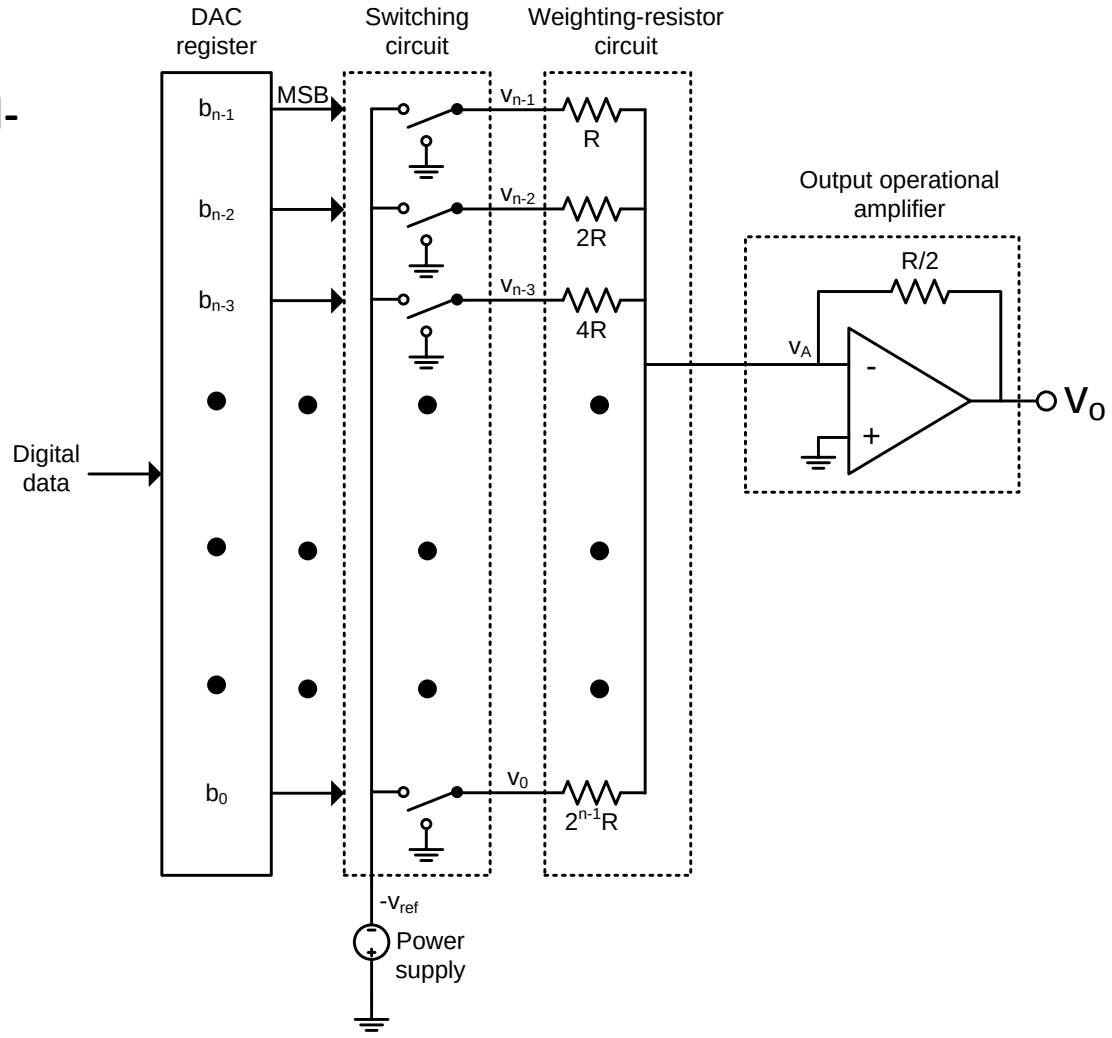
$$FSV = \left( 1 + \frac{1}{2} + \ldots + \frac{1}{2^{n-1}} \right) \frac{v_{ref}}{2}$$

- use geometric series

$$1 + r + r^2 + \ldots + r^{n-1} = \frac{1 - r^n}{1 - r}$$

- gives

$$FSV = \left( 1 - \frac{1}{2^n} \right) v_{ref}$$

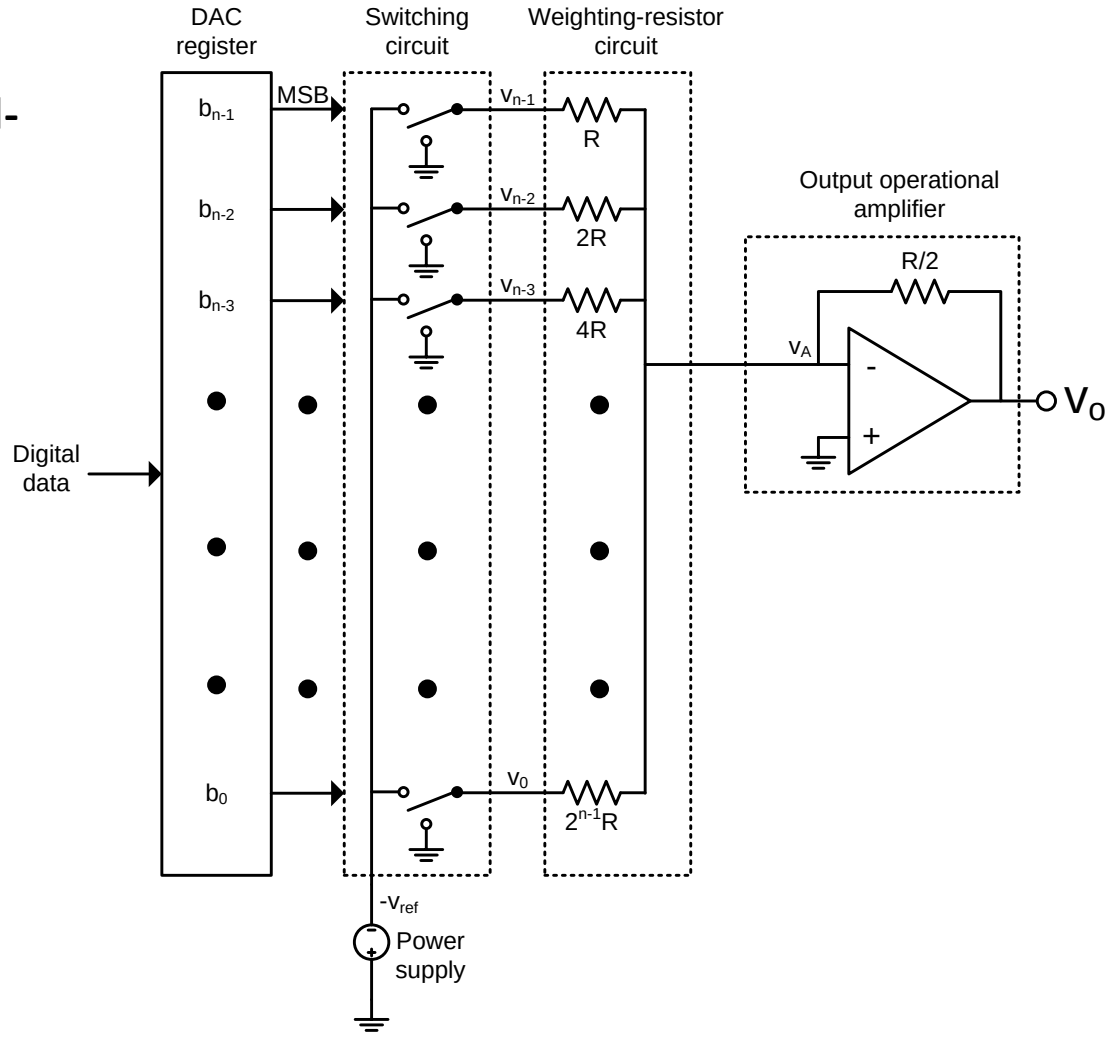


# Weighted-resistor DAC

- **what is the output voltage Vo of the weighted-resistor DAC when all bits are equal to 1?**

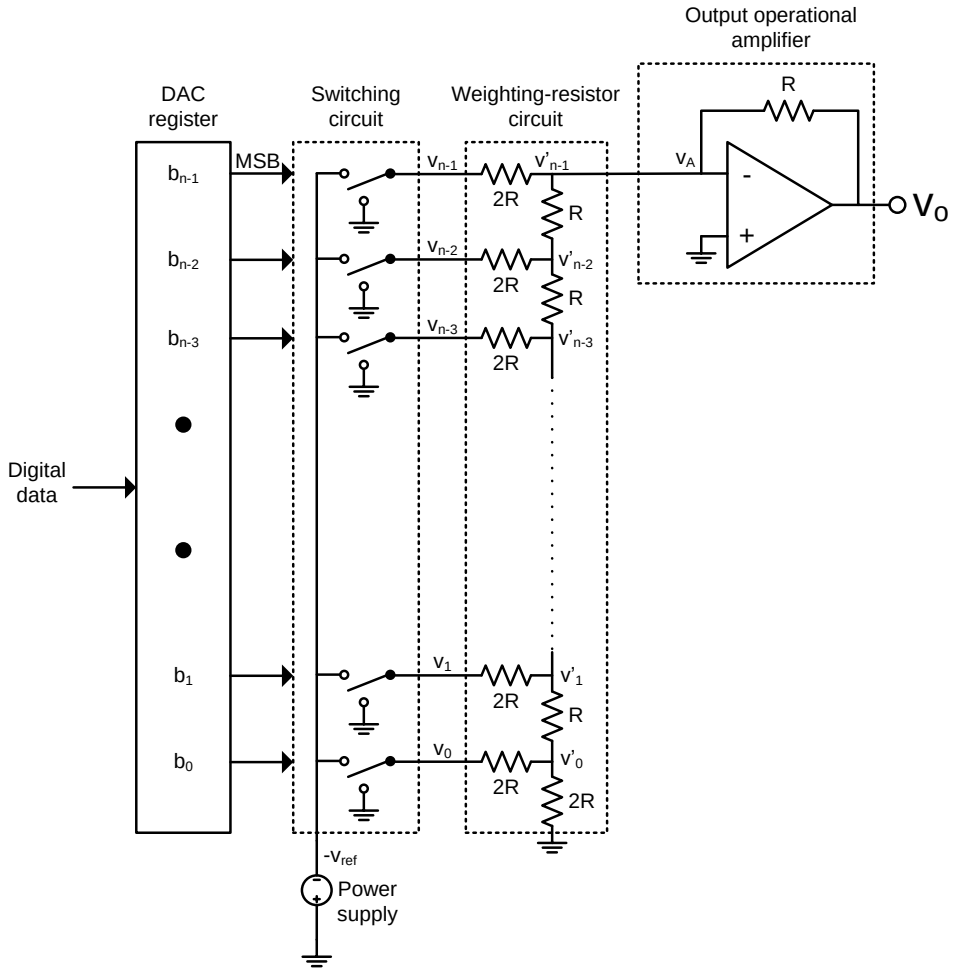
$$FSV = \left(1 - \frac{1}{2^n}\right) v_{ref}$$

- full scale output voltage is smaller then $v_{ref}$
- error is negligible if n is large enough



# Ladder DAC

- different resistor values in weighted-resistor DAC hard to produce
- ladder DAC provides alternative with only two resistor values
- **what is the output voltage $V_o$ of the ladder DAC in terms of the input bits (digital data – $b_i$)?**



# Ladder DAC

- **what is the output voltage $V_o$ of the ladder DAC in terms of the input bits (digital data – $b_i$)?**
- apply KCL at node i

$$\frac{v_i - v'_i}{2R} + \frac{v'_{i+1} - v'_i}{R} + \frac{v_{i-1} - v'_i}{R} = 0$$

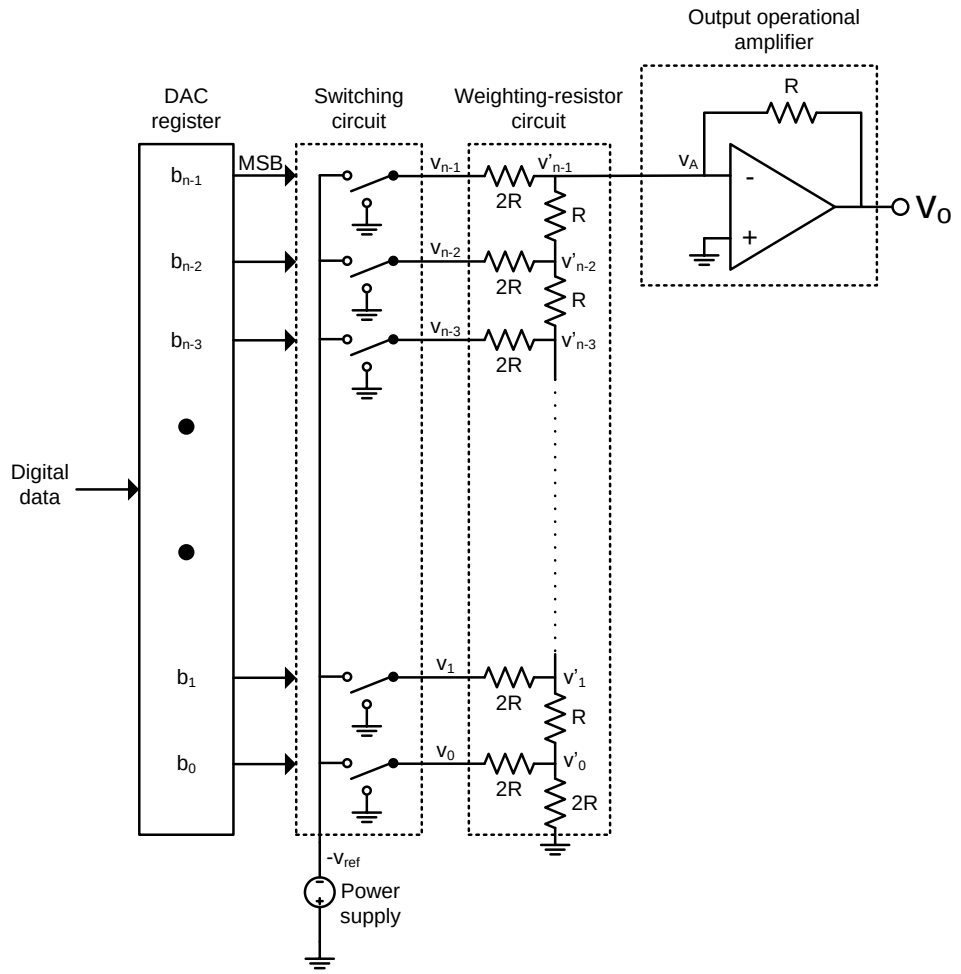
- for all nodes except nodes 0 and n-1 this can be written as

$$\frac{1}{2}v_i = \frac{5}{2}v'_i - v'_{i-1} - v'_{i+1}$$

- for node 0 holds

$$\frac{v_0 - v'_0}{2R} + \frac{v'_1 - v'_0}{R} + \frac{0 - v'_0}{2R} = 0$$

$$\Rightarrow \frac{1}{2}v_0 = 2v'_0 - v'_1$$



# Ladder DAC

- **what is the output voltage $V_o$ of the ladder DAC in terms of the input bits (digital data – $b_i$)?**
- for node n-1 holds

$$\frac{v_{n-1} - v'_{n-1}}{2R} + \frac{v'_{out} - v'_{n-1}}{R} + \frac{v'_{n-2} - v'_{n-1}}{R} = 0$$

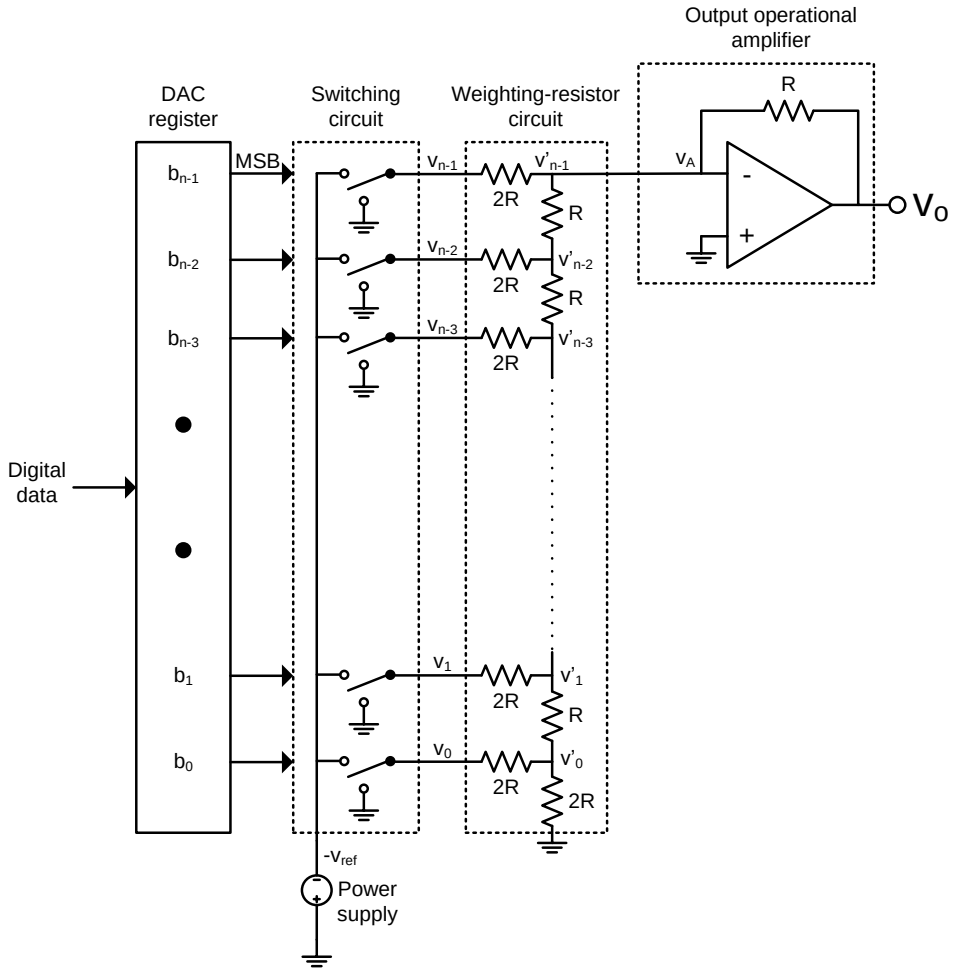
- it holds that

$$v'_{n-1} = 0$$

- hence

$$\frac{v_{n-1}}{2R} + \frac{v_{out}}{R} + \frac{v'_{n-2}}{R} = 0$$

$$\Rightarrow \frac{1}{2} v_{n-1} = -v_{out} - v'_{n-2}$$



# Ladder DAC

- **what is the output voltage $V_o$ of the ladder DAC in terms of the input bits (digital data – $b_i$)?**
- summary
  - for node i (except 0 and n-1) holds

$$\frac{1}{2}v_i = \frac{5}{2}v'_i - v'_{i-1} - v'_{i+1}$$

  - for node 0 holds

$$\frac{1}{2}v_0 = 2v'_0 - v'_1$$

  - for node n-1 holds

$$\frac{1}{2}v_{n-1} = -v_{out} - v'_{n-2}$$

- combine these equations while using $v'_{n-1}=0$

# Ladder DAC

- **what is the output voltage $V_o$ of the ladder DAC in terms of the input bits (digital data – $b_i$)?**
- combine these equations while using $v'_{n-1}=0$

$$\frac{1}{2}v_{n-1} = -v_{out} - v'_{n-2}$$

$$\frac{1}{2^2}v_{n-2} = \frac{1}{2}\frac{5}{2}v'_{n-2} - \frac{1}{2}v'_{n-3}$$

$$\frac{1}{2^3}v_i = \frac{1}{2^2}\frac{5}{2}v'_{n-3} - \frac{1}{2^2}v'_{n-4} - \frac{1}{2^2}v'_{n-2}$$

$$\frac{1}{2^{n-1}}v_0 = \frac{1}{2^{n-2}}\frac{5}{2}v'_0 - \frac{1}{2^{n-2}}v'_0 - \frac{1}{2^{n-2}}v'_2$$

$$\frac{1}{2^2}\frac{1}{2}v_0 = \frac{1}{2^{n-1}}2v'_0 - \frac{1}{2^{n-1}}v'_1$$

- sum these n equations

$$\frac{1}{2}v_{n-1} + \frac{1}{2^2}v_{n-2} + \frac{1}{2^3}v_{n-3} + \ldots + \frac{1}{2^n}v_0 = -v_{out}$$

# Ladder DAC

- **what is the output voltage $V_o$ of the ladder DAC in terms of the input bits (digital data – $b_i$)?**
- sum these n equations

$$\frac{1}{2}v_{n-1}+\frac{1}{2^2}v_{n-2}+\frac{1}{2^3}v_{n-3}+\ldots+\frac{1}{2^n}v_0=-v_{out}$$

- use $v_i = -b_i\, v_{ref}$

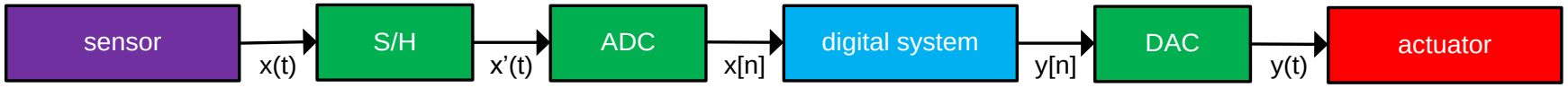
$$v_{out}=\left(\frac{1}{2}b_{n-1}+\frac{1}{2^2}b_{n-2}+\frac{1}{2^3}b_{n-3}+\ldots+\frac{1}{2^n}b_0\right)v_{ref}$$

- output voltage is identical to result for the weighted-resistor DAC
- result realized with fewer resistor values (easier to manufacture)

# Analog signals and digital systems

- digital system works on digitized samples of the signal


- connecting the analog and digital world




  - S/H – sample and hold circuit
  - ADC – analog to digital conversion
  - DAC – digital to analog conversion

# Analog to digital conversion

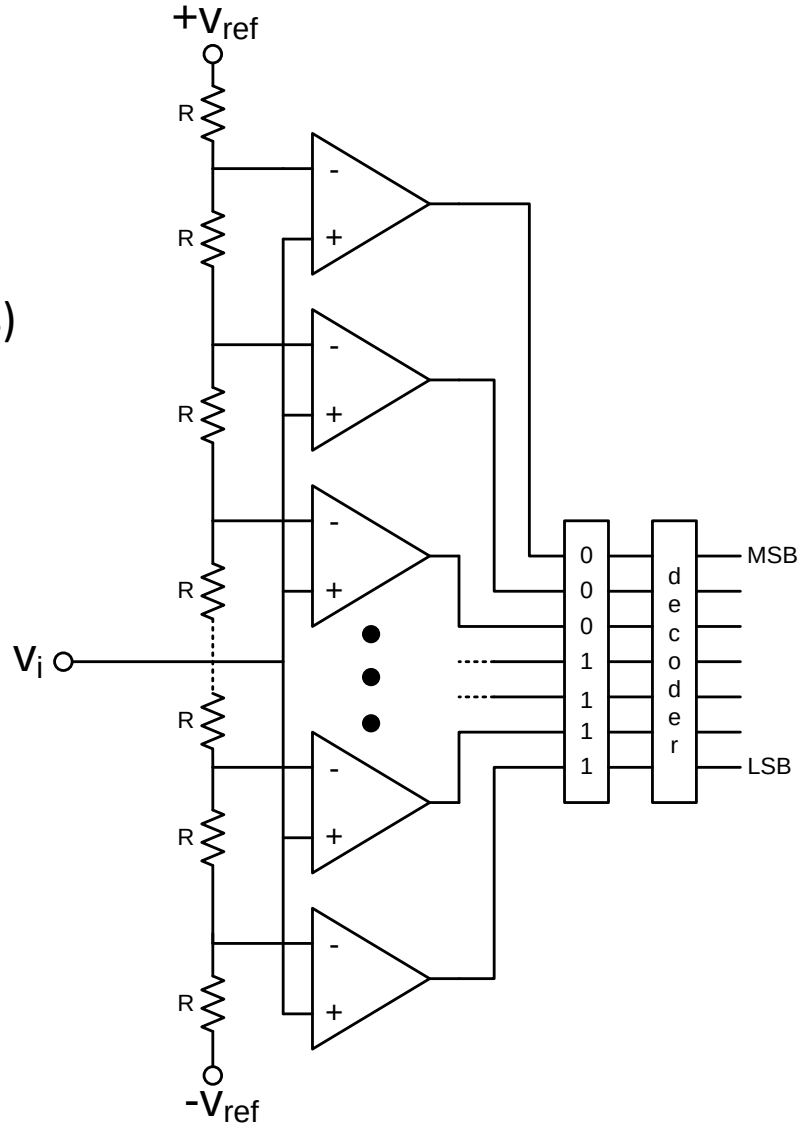
- several different ADC implementations are used in practical system
- most important characteristics
  - time needed for conversion
  - amount of hardware needed

- three commonly used types and their differences (speed, area)
  - flash ADC (fastest, large)
  - dual-slope ADC (slow, small)
  - successive approximation ADC (fast, medium)

# Flash ADC

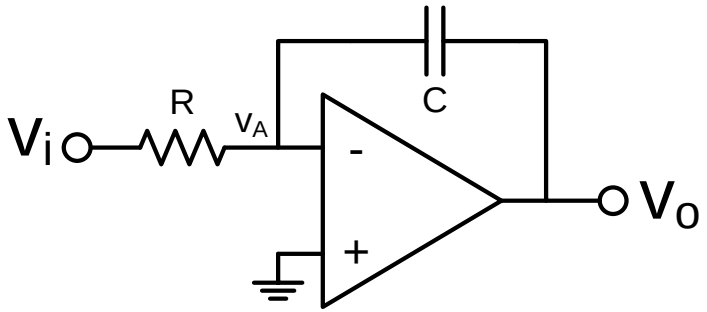
- resistive divider with $2^N$ resistors
- divider provides reference voltages
- comparators output 1 when $v_i$ above reference voltage or 0 otherwise
- code at output of comparators known as digital thermometer code
- decoder translates code to digital value (using inverters and NAND gates)

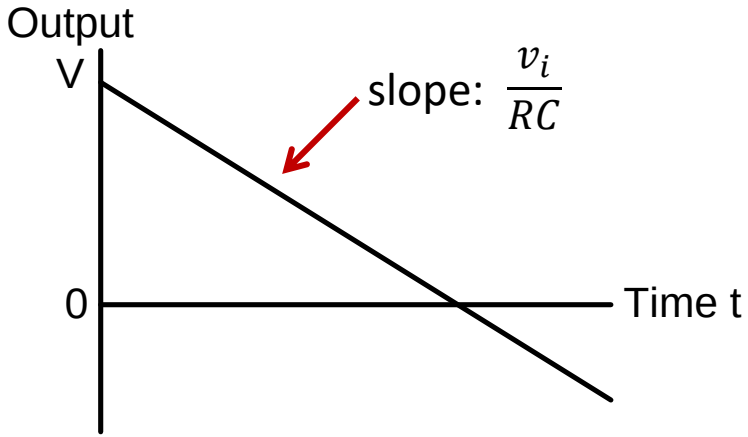
- pro's and con's
  - fast
  - many comparators required



# Dual-slope ADC

- dual-slope ADC based operation of RC integrating circuit



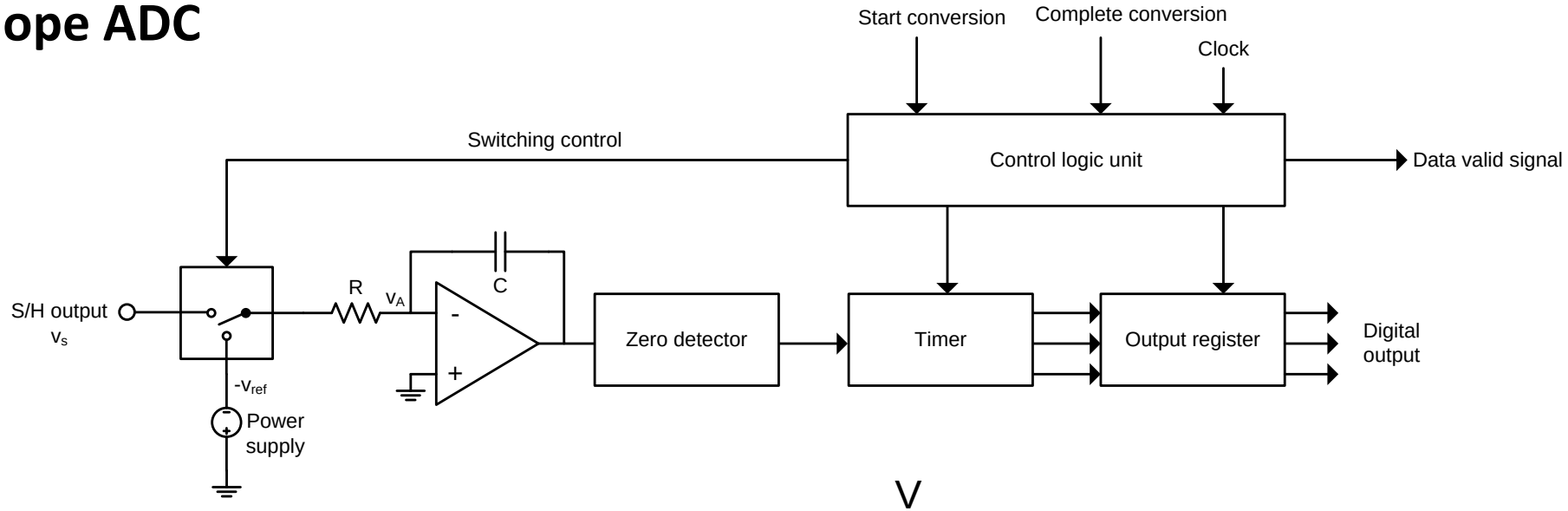



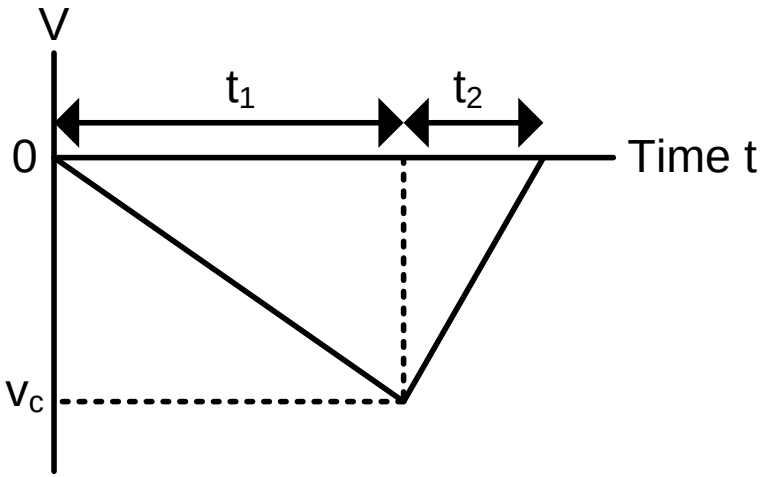

- **what is the output voltage $v_o(t)$ of the integrating circuit?**
  - it holds that voltage $V_A = 0$
  - input voltage $v_i$ is constant over time
  - using KCL

$$\frac{v_i}{R} + C\frac{dv_o}{dt} = 0 \Rightarrow v_o(t) = v_o(0) - \frac{v_i \cdot t}{RC}$$

  - slope of curve proportional to input voltage $v_i$

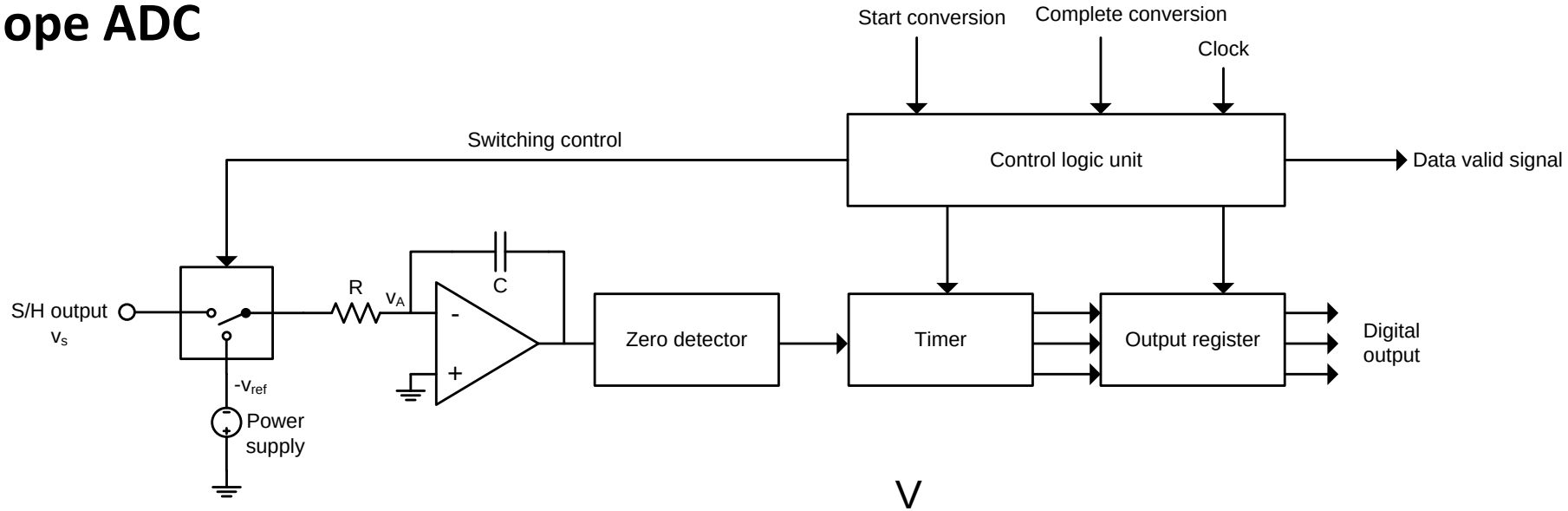
# Dual-slope ADC

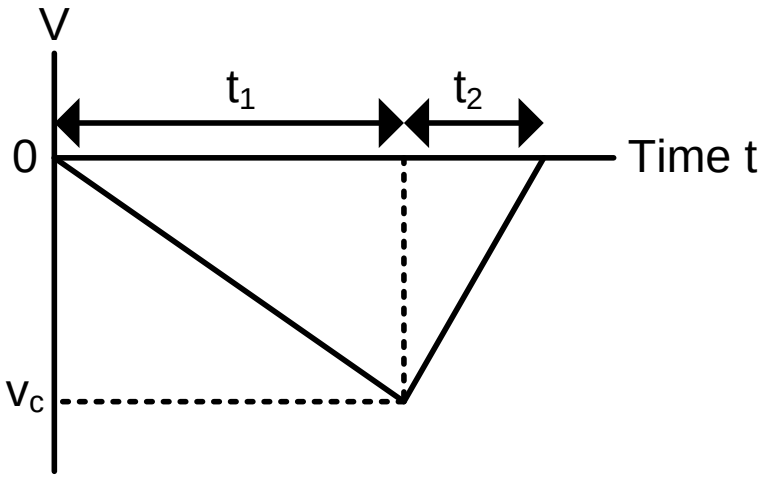



- operation
- initially capacitor C is discharged (zero voltage)
- voltage $v_s$ applied to input of switch
- start conversion signal applied
  - timer reset to zero
  - output register reset to zero
  - voltage $v_s$ applied to integrating circuit

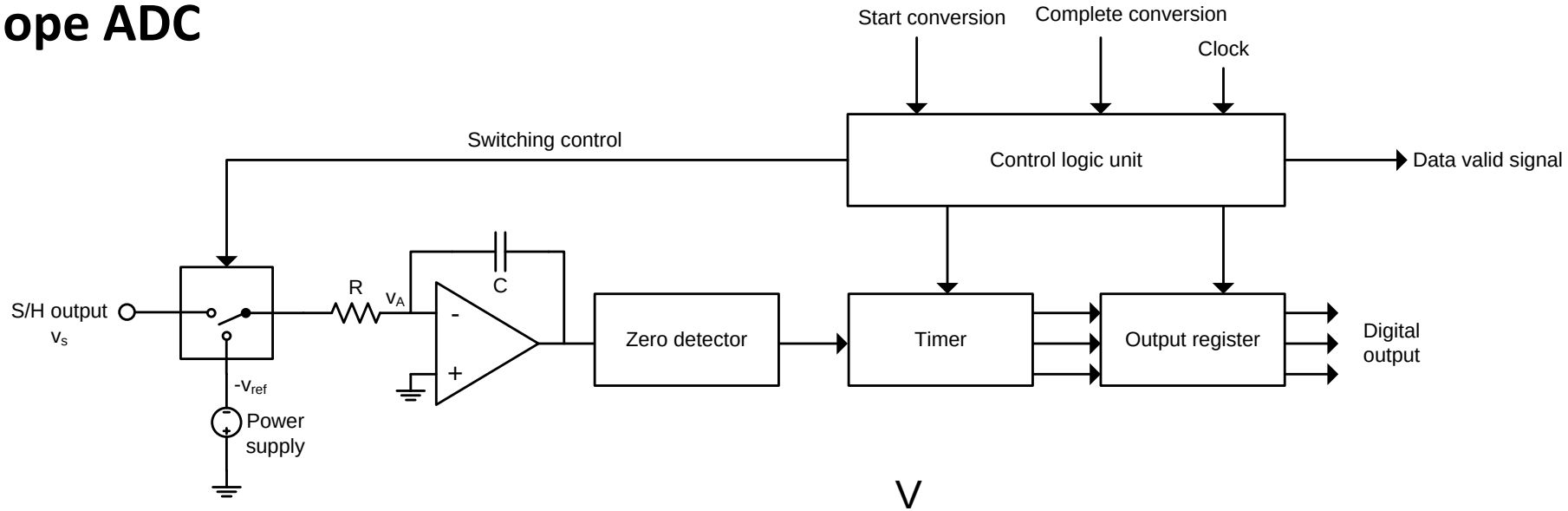
# Dual-slope ADC



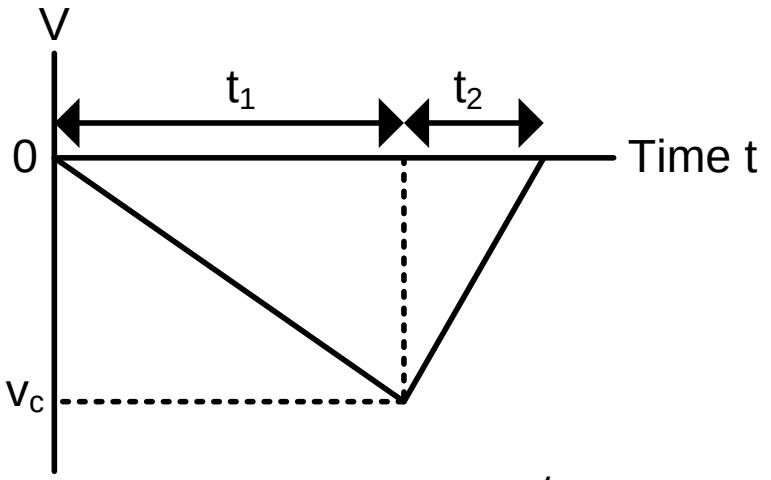

- operation
- after time $t_1$ ($n_1$ clock cycles)
  - switch input integrating circuit to $-v_{ref}$
  - clear timer and start timing (counting) again
- capacitor is discharging
- zero detector (comparator) detects zero crossing and stops timer at time $t_2$ ($n_2$ clock cycles)

# Dual-slope ADC




- $v_o$ of integrating circuit

$$v_o(t) = v_o(0) - \frac{v_i \cdot t}{RC}$$

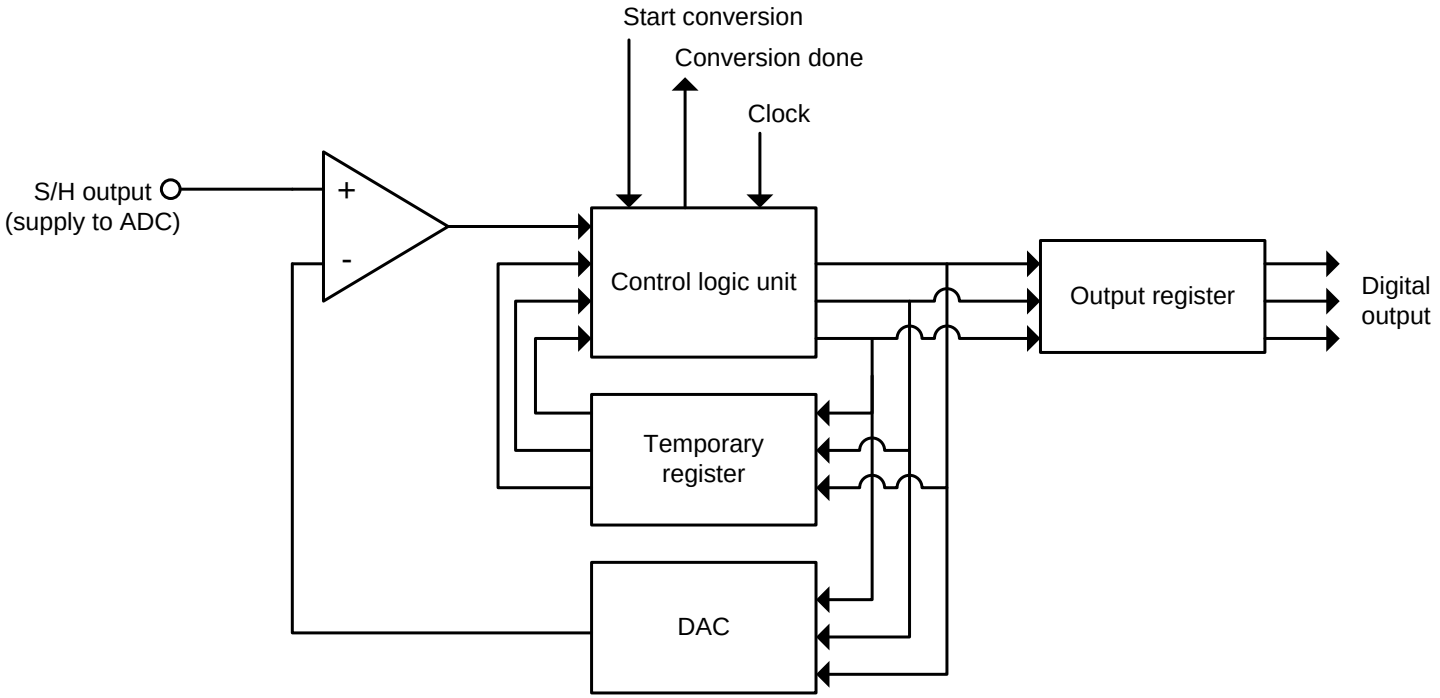


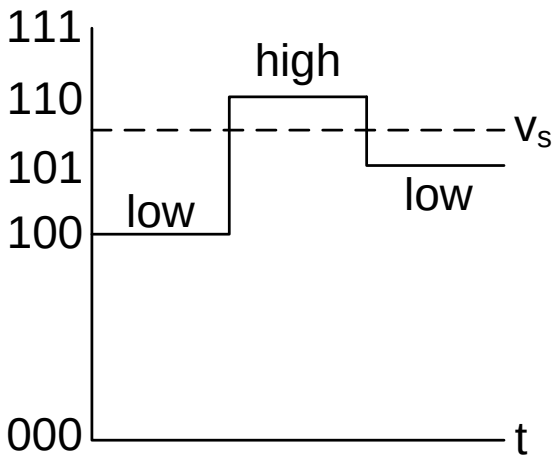

- at $t_1$ it holds $-v_c = 0 - \frac{v_s \cdot t_1}{RC} \Leftrightarrow v_c = \frac{v_s \cdot t_1}{RC}$
- at $t_2$ it holds $0 = -v_c + \frac{v_{ref} \cdot t_2}{RC} \Leftrightarrow v_c = \frac{v_{ref} \cdot t_2}{RC}$

$$\Rightarrow v_s \cdot t_1 = v_{ref} \cdot t_2 \Leftrightarrow v_s = v_{ref} \frac{t_2}{t_1} = v_{ref} \frac{n_2}{n_1} = \frac{v_{ref}}{n_1} n_2$$

- $v_{ref}$ and $n_1$ are fixed; $v_s$ proportional to $n_2$

# Successive-approximation ADC

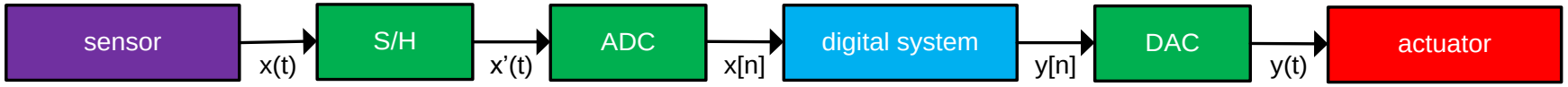


# Analog signals and digital systems

- digital system works on digitized samples of the signal

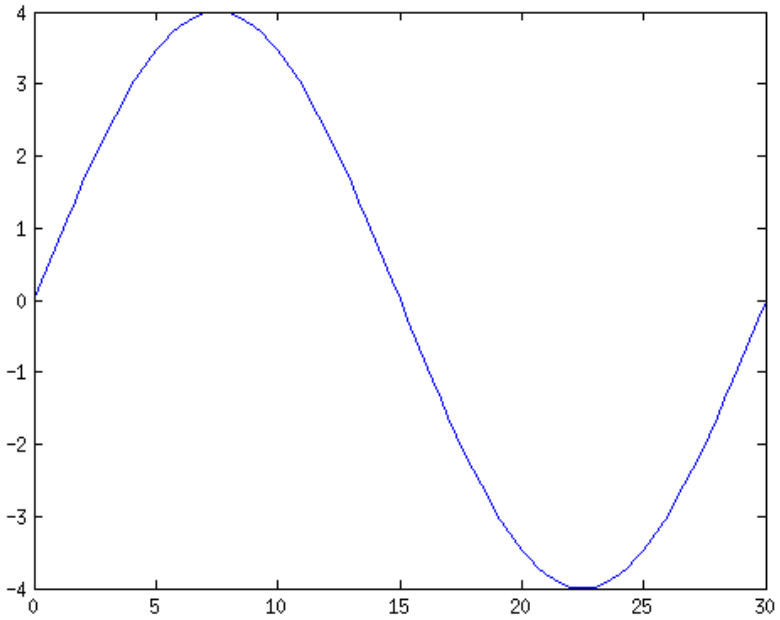

- connecting the analog and digital world




  - S/H – sample and hold circuit
  - ADC – analog to digital conversion
  - DAC – digital to analog conversion

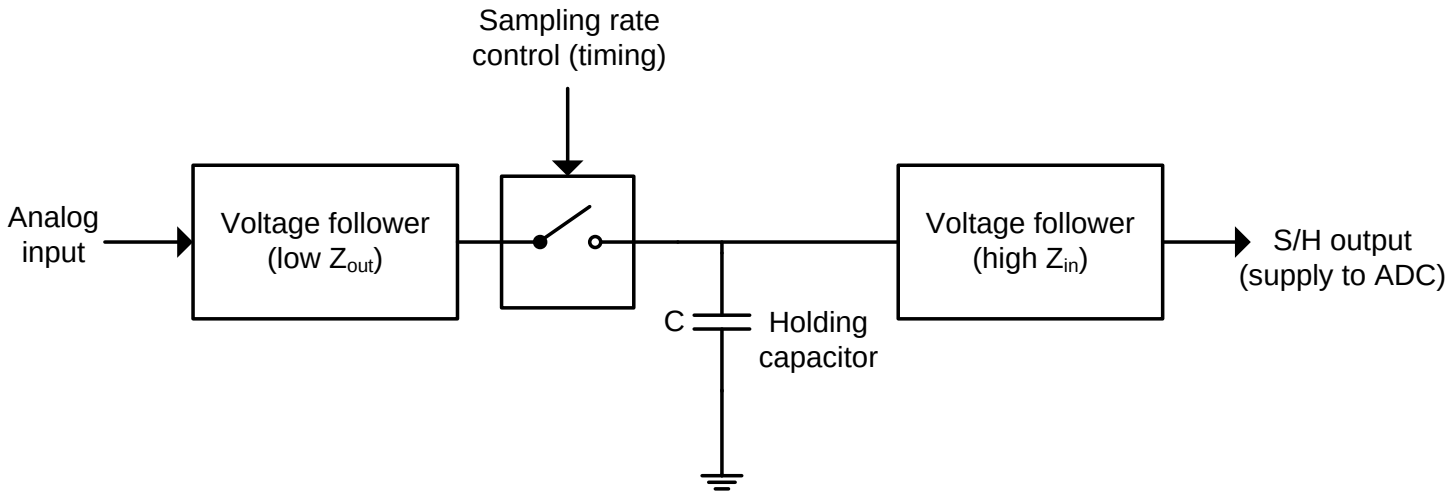
# Sample and hold circuit

- analog to digital conversion takes time
- continuous signal may change value during conversion process



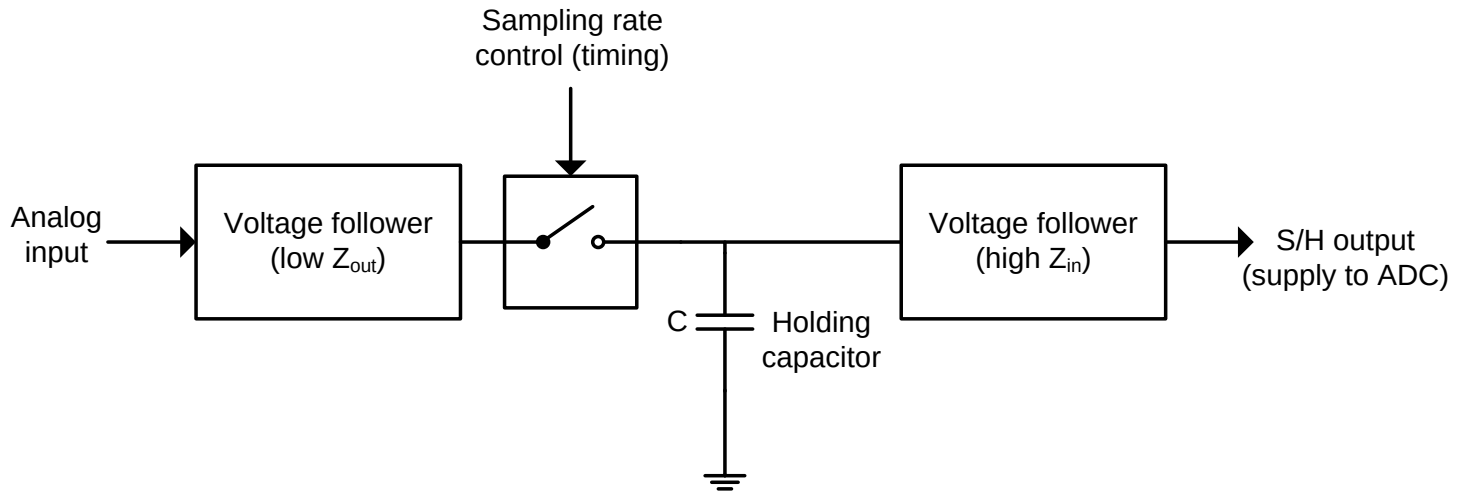

- stable (constant) value must be provided to ADC
- solution: use sample and hold circuit

# Sample and hold circuit

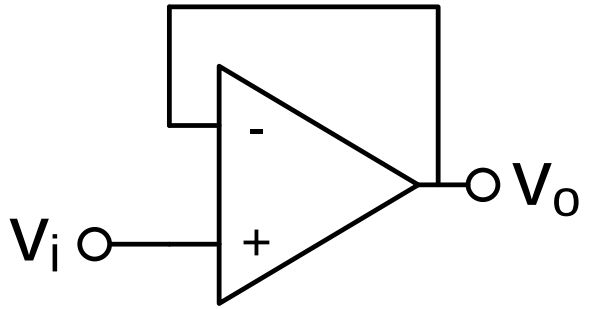



- concept
  - charge holding capacitor to voltage of analog signal
- requirements
  - charging needs to be done quickly
  - charge needs to stay on capacitor during ADC

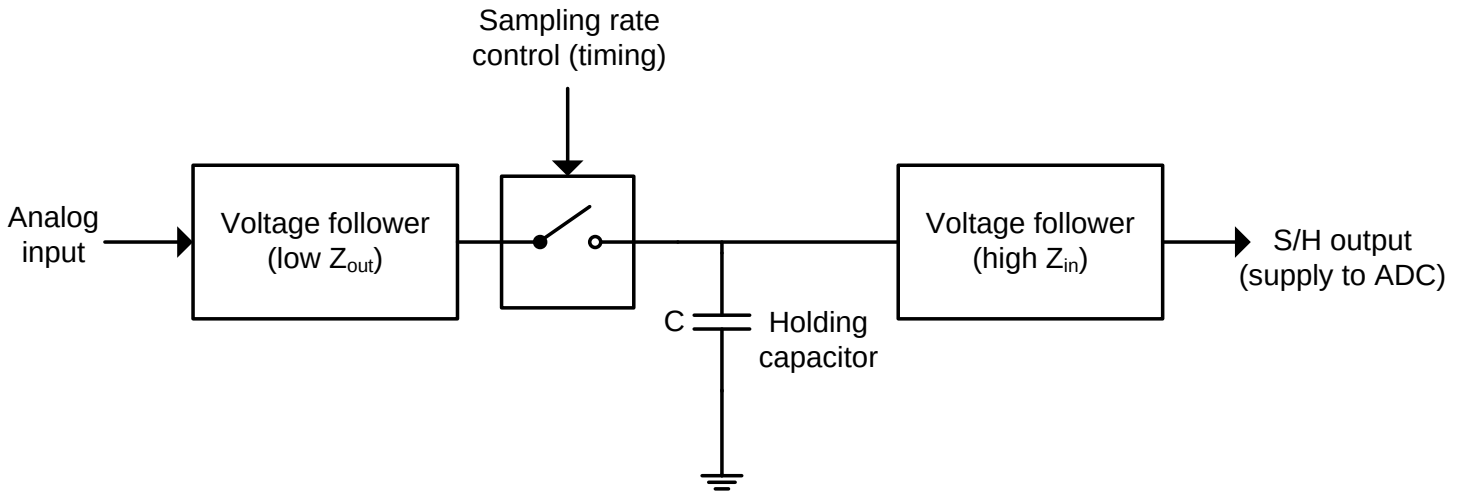
# Sample and hold circuit



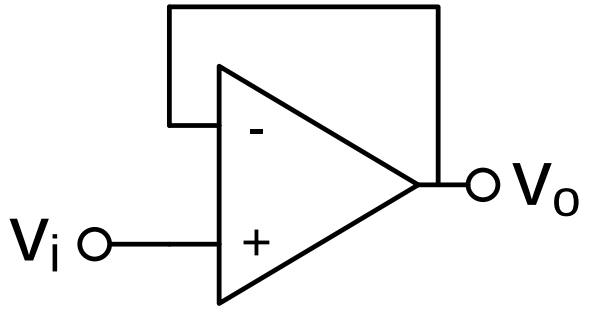

- requirement: charging needs to be done quickly
  - charging time constant $\tau_s = R_s C$
    - capacitance C fixed because of holding requirement (typically ~100 pF)
  - to get a small τs, the source resistance Rs must be small
  - use voltage follower with low output impedance
    - output voltage $v_o = v_i$
    - op-amp has low output impedance



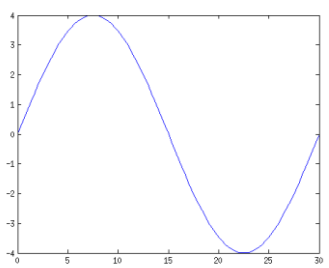
# Sample and hold circuit

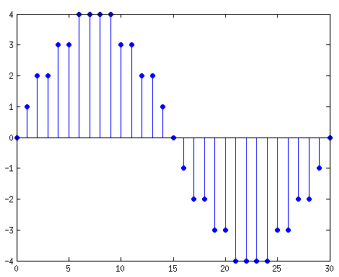


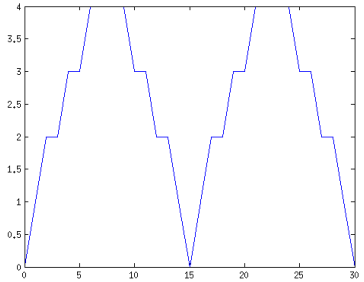

- requirement: charge needs to stay on capacitor during ADC
  - circuit connected to holding capacitor must have high input impedance
  - use voltage follower which has high input impedance

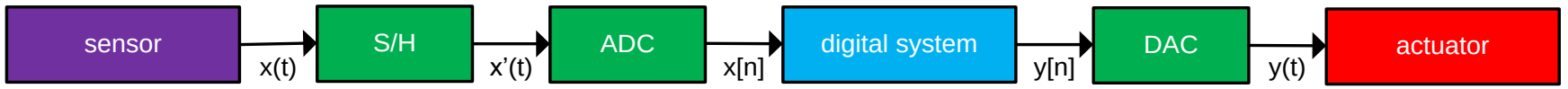


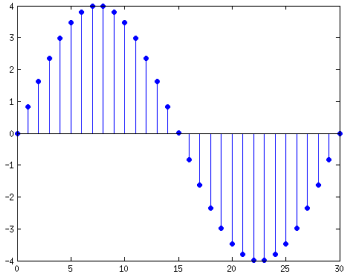
# Analog signals and digital systems

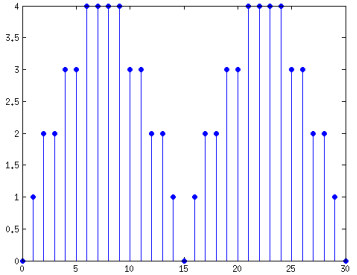










- S/H – sample and hold circuit
- ADC – analog to digital conversion
- DAC – digital to analog conversion