PreMaDoNa

Track 2: NoC implementation

The Physical view

Premadonna meeting 15-10-2004

Vision: evolutionary view

An NoC architecture provides the following advantages:

- Simplification of the IP interfaces
  (due to higher design abstraction and restricted design space)
  - enabling simpler composability of hardware
  - enabling better and more reuse
- Early predictability of performance
- Natural division into synchronous areas

Most likely, an NoC does not:

- result in the cheapest, smallest, (power-) efficient parts
- reduce mask costs

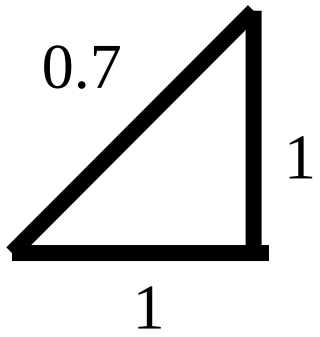
Goals

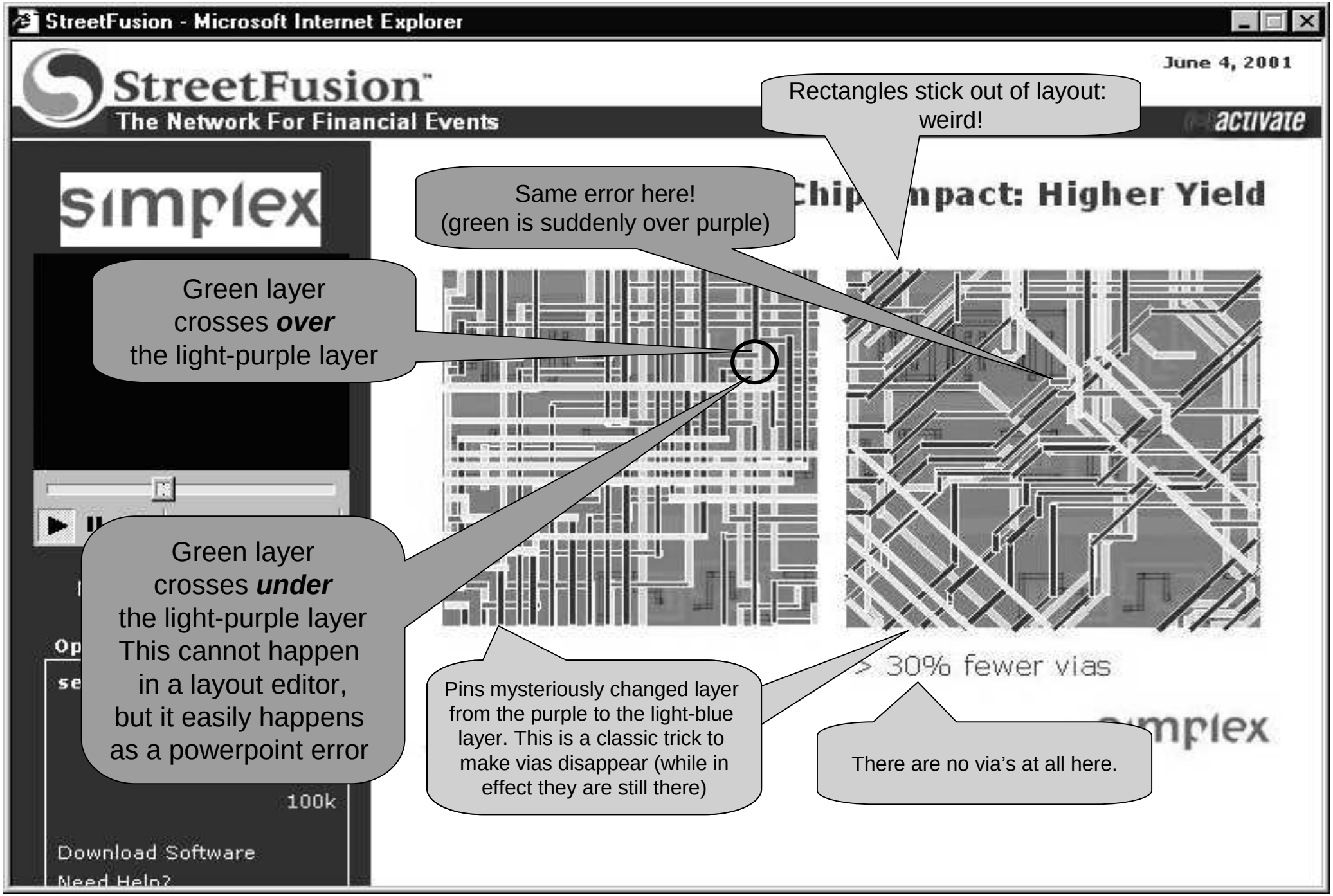
- Explore the physical issues:
  - Expose opportunities as well as weaknesses.
  - Explore sweet-spots and trade-offs.
  - Stuff that simulation at model-level cannot expose.
- Result: a demonstration of the physical feasibility
- Result: insight in cost-benefit of an SoC system, where previous efforts have stalled
  - Easy of use of the methodology
  - Area & Power overhead
  - Dimensioning of the network

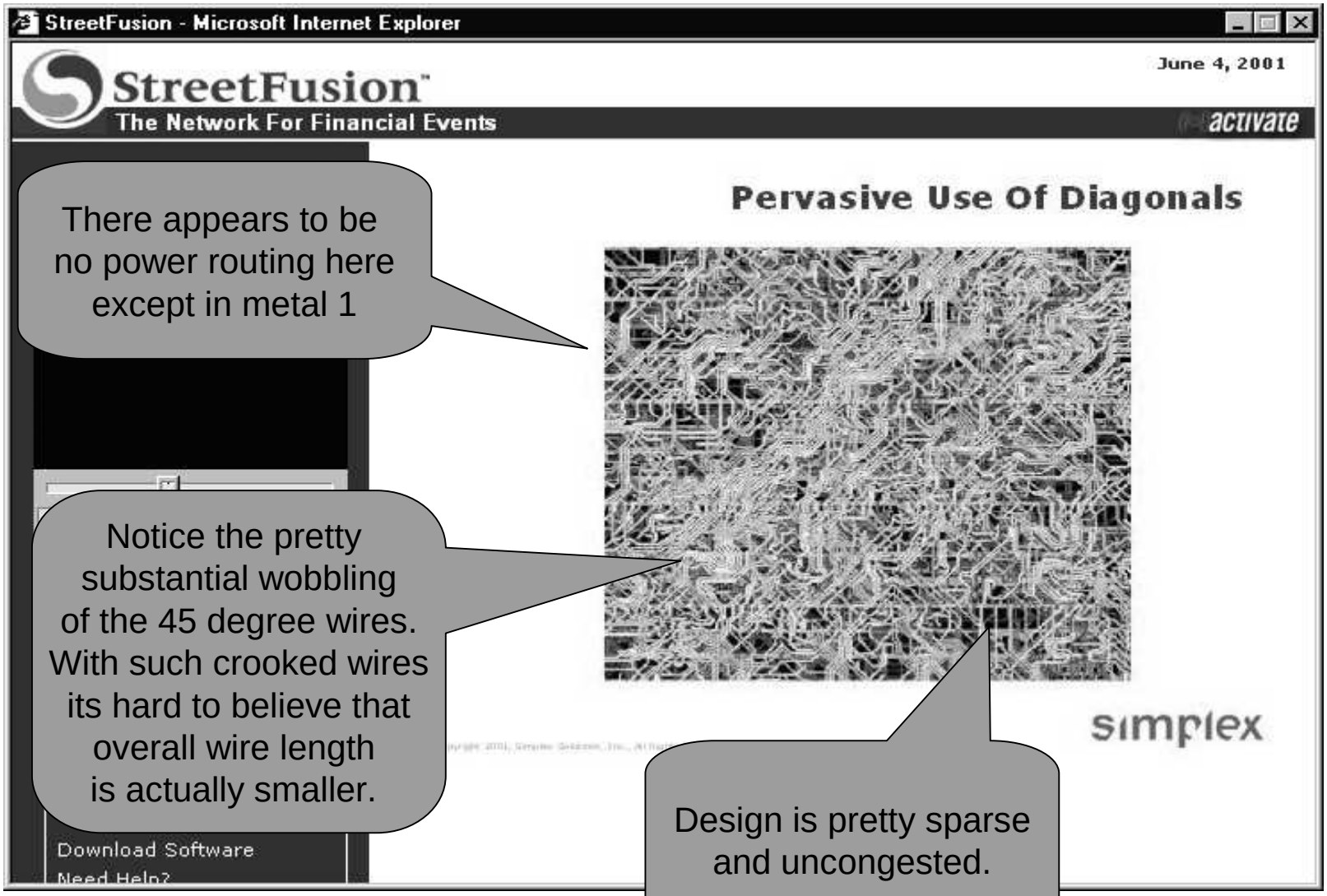
An Analogy: the X-architecture

Key idea here: instead of routing orthogonally, put some layers under 45 degree angle

Goal: shorter wires




StreetFusion - Microsoft Internet Explorer
StreetFusion
The Network For Financial Events
June 4, 2001
activate
simplex
Rectangles stick out of layout: weird!
Same error here! (green is suddenly over purple)
Green layer crosses over the light-purple layer
Green layer crosses under the light-purple layer This cannot happen in a layout editor, but it easily happens as a powerpoint error
Pins mysteriously changed layer from the purple to the light-blue layer. This is a classic trick to make vias disappear (while in effect they are still there)
There are no via's at all here.
> 30% fewer vias
100k
Download Software
Need Help?


StreetFusion - Microsoft Internet Explorer
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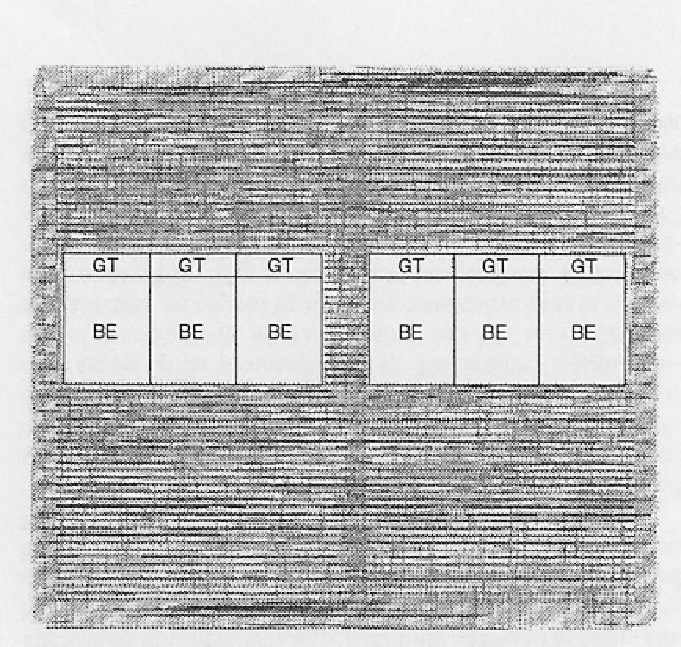
activate
Pervasive Use Of Diagonals
There appears to be no power routing here except in metal 1
Notice the pretty substantial wobbling of the 45 degree wires. With such crooked wires its hard to believe that overall wire length is actually smaller.
Design is pretty sparse and uncongested.
simplex
Download Software
Need Help?

Previous work

- 2 chips at Philips
  - –Router
  - –Chip with 4 routers and traffic generators
- Common characteristics:
  - –Straight ‘flat’ implementation: a sea of gates
  - –Physical size and arrangement of the blocks is not taken into account

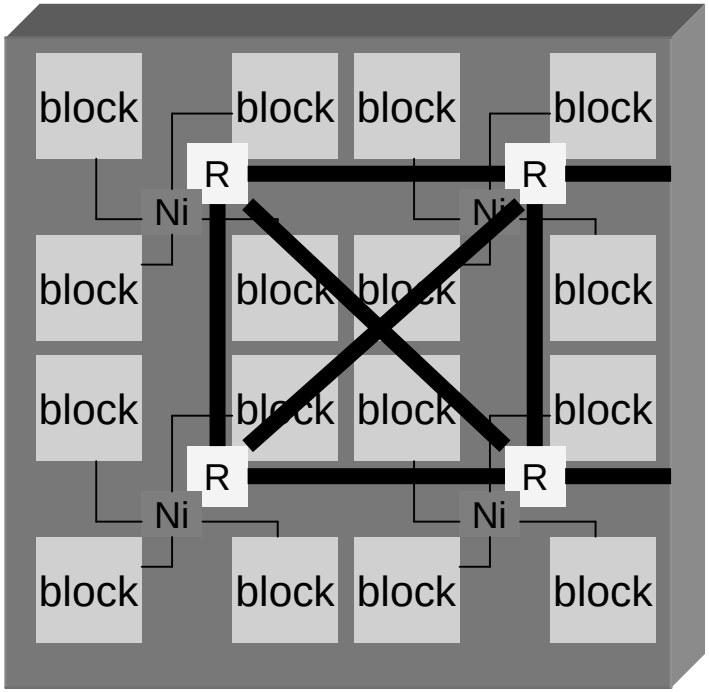


Big questions

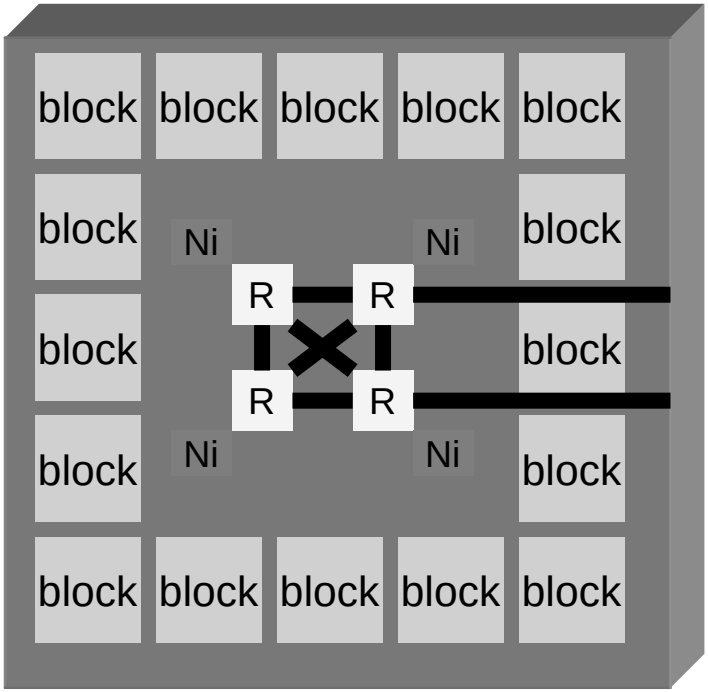
NoC Floorplan template determines everything!

- Size of the blocks
- Block size variability
- Length of communication channels between routers
- Power consumption
    - result of chip area
    - overhead in network encoding of data

Finding a chip floorplan



mesh

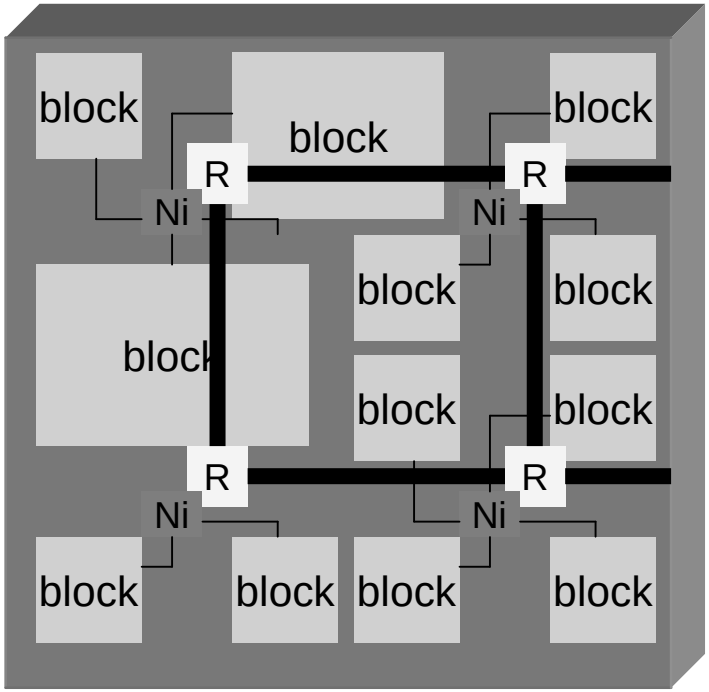


star

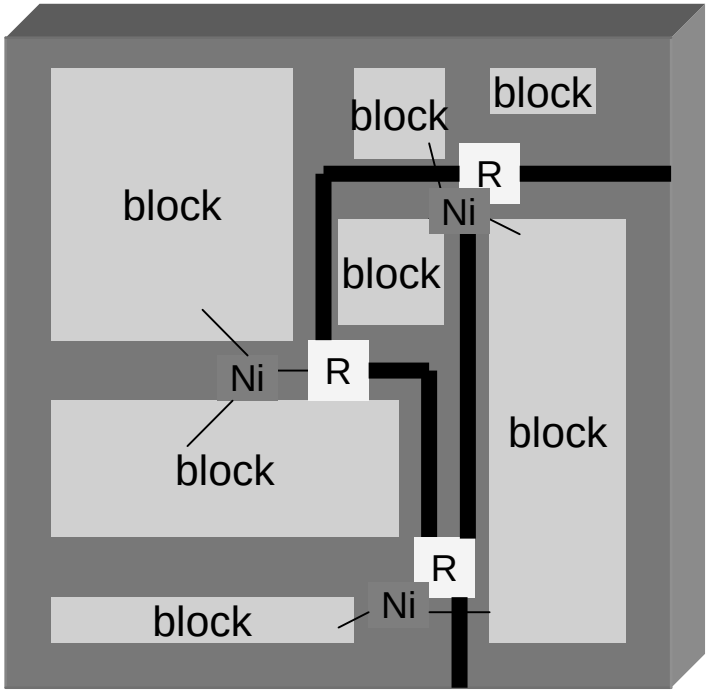
Assumption: Routers, wiring and blocks are different physical entities

Goal: simple generator, explore alternatives

Non-uniform blocks, non-homogeneous designs



Semi-regular



irregular

Assumption: Routers, wiring and blocks are different physical entities

Goal: simple generator

Components

R 1. Router: Philips design

   1. Re-use material, including FiFo's

Ni 2. Network interface

   1. Re-use philips

3. Inter-router wiring

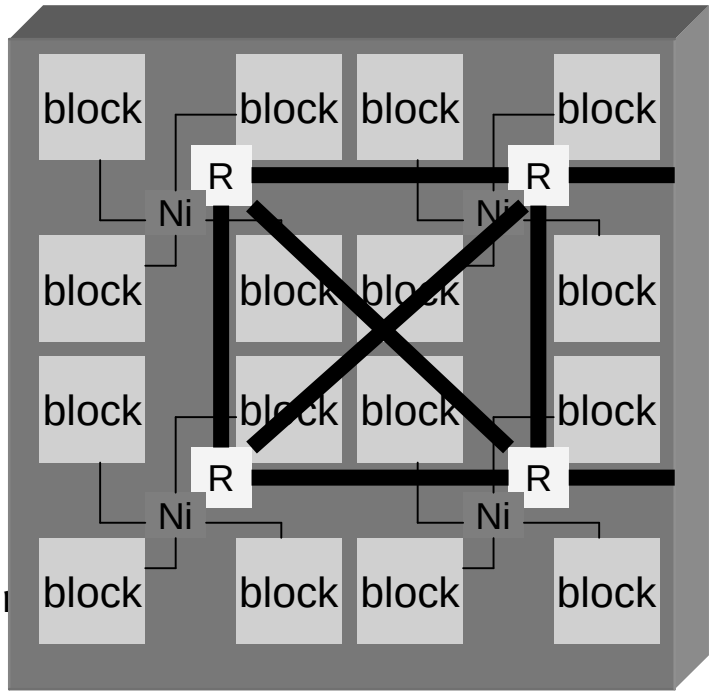
   1. Normal wires, or generator for specialized high-per

block 4. Blocks

   1. Realistic size! But re-use simple traffic generators (keeps chips smaller)
   2. Using a real applications is probably a lot more work.

5. Process, library: same Philips/TSMC .13

6. Design tool: Magma and/or Cadence.



Approach

This is a multi-dimensional puzzle where we have to find a feasible spot.

1. Explore a limited number of floorplans.
   - Back-of-the-envelope calculations for delay for each
- Pick feasible one.
- Decide how to implement communication channels
- Write generator program for the floor plan.

Open questions

• When to spread blocks between routers, when to use the ‘shortcut’ in the network interface?

•Dimensioning mechanism for the bandwidth.