PHILIPS

NoC Setup on FPGA

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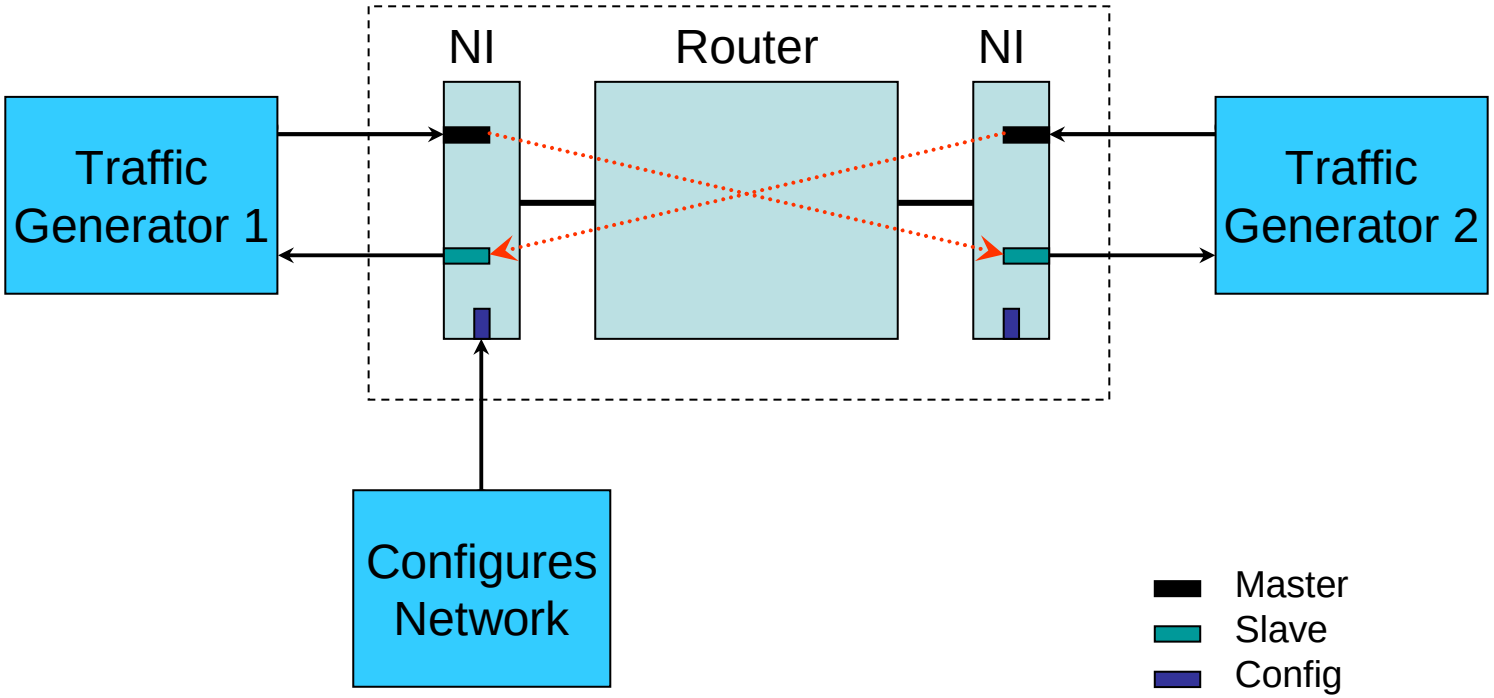
Outline

- Network Topology
- Design Flow
- Testing and Debugging
- FPGA Resource Utilisation
- Performance Metrics
- Demonstration
- Discussion Topics

Network Topology



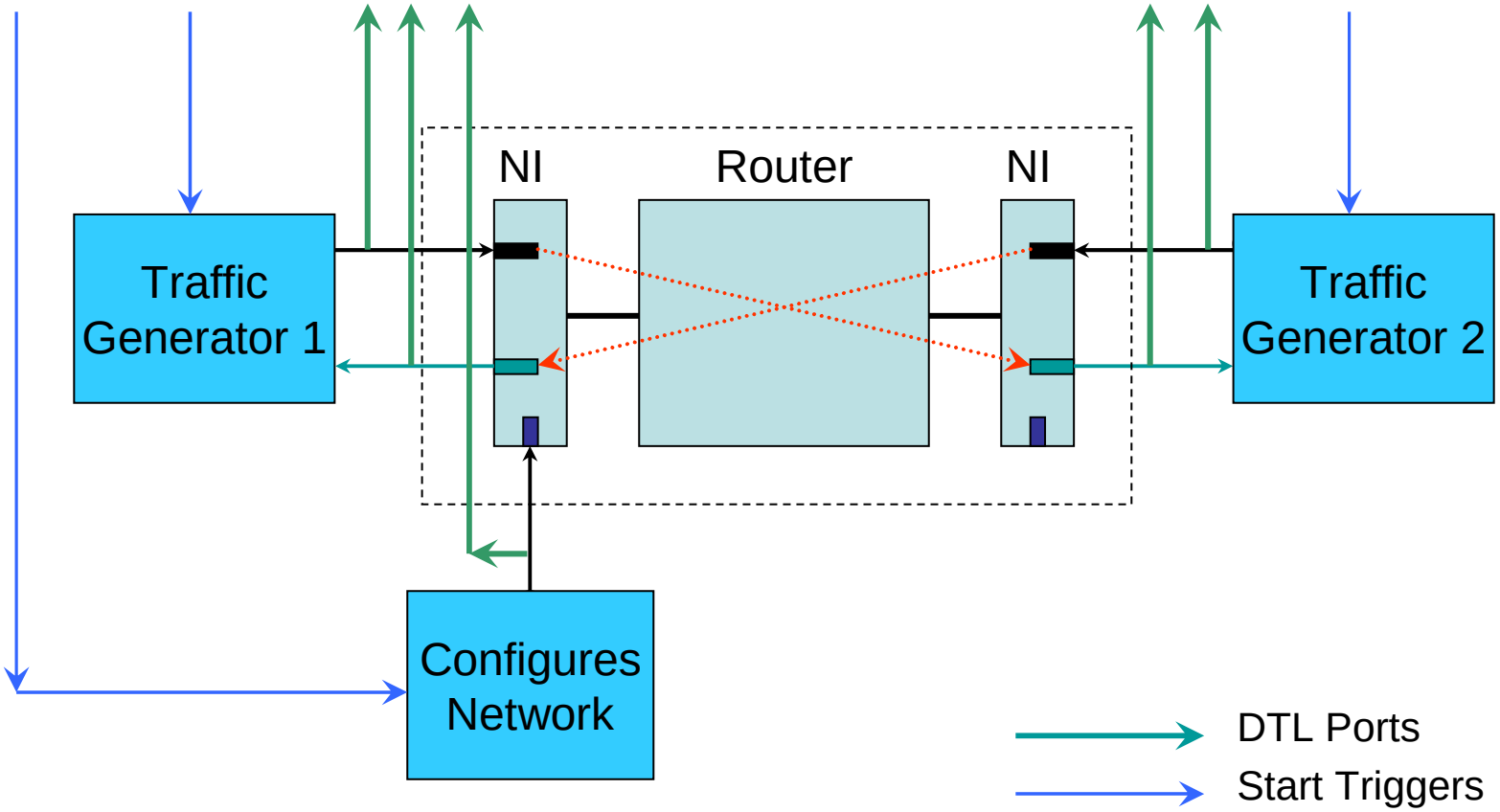
Design Flow

- Test independent models of processors and network
- Replace tcl-scripts with processors one at a time in the network and simulate
- Synthesize the design, place and route, and program the FPGA
- Test using Logic Analyzer and Chipscope
- Compare with simulation

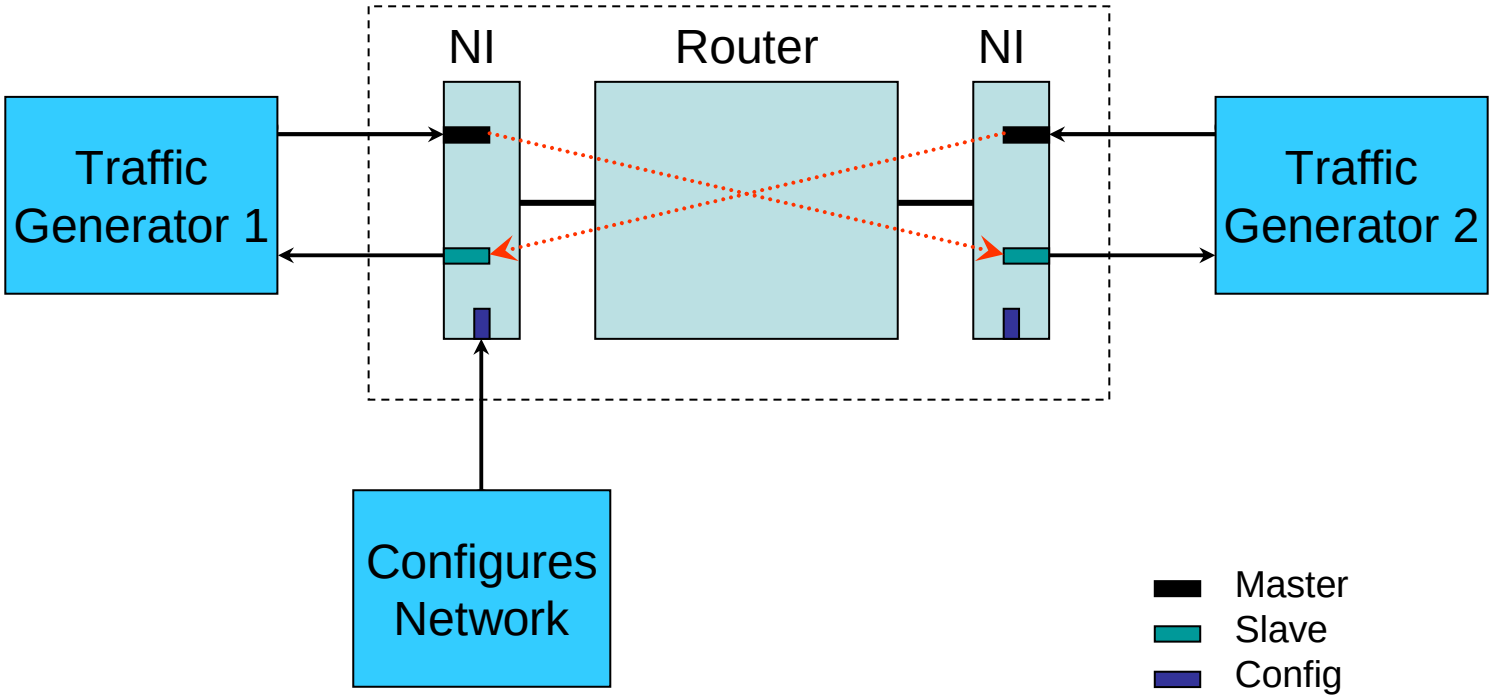
Design Flow – Network Configurator

- Preprocessing the C-code
  - Reduces the final code-size to one-third: saves memory
  - Much faster in execution

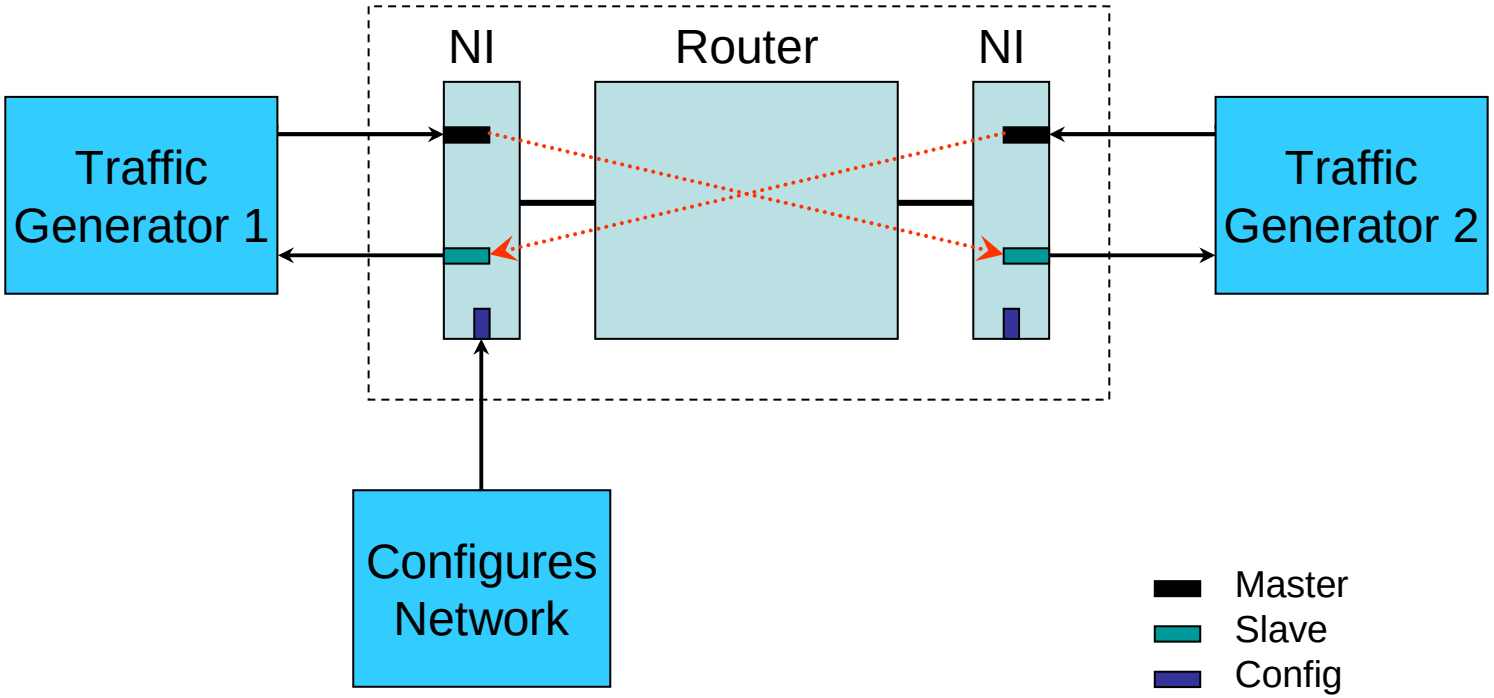
Testing and Debugging



Testing and Debugging – Scenario 1



Testing and Debugging – Scenario 2



FPGA Resource Utilisation

- Xilinx Virtex2 6000:
  - 72,000 Logic Cells (LCs)
  - 144*16 Kbits RAM each
- Moustique: 20% LCs, 8-13 Block RAMs
- Network: 7% LCs
- Total: 71% LCs, 29 Block RAMs
- Chipscope: 61 Block RAMs
  - 60 samples, depth of 16,384 each

Performance Metrics

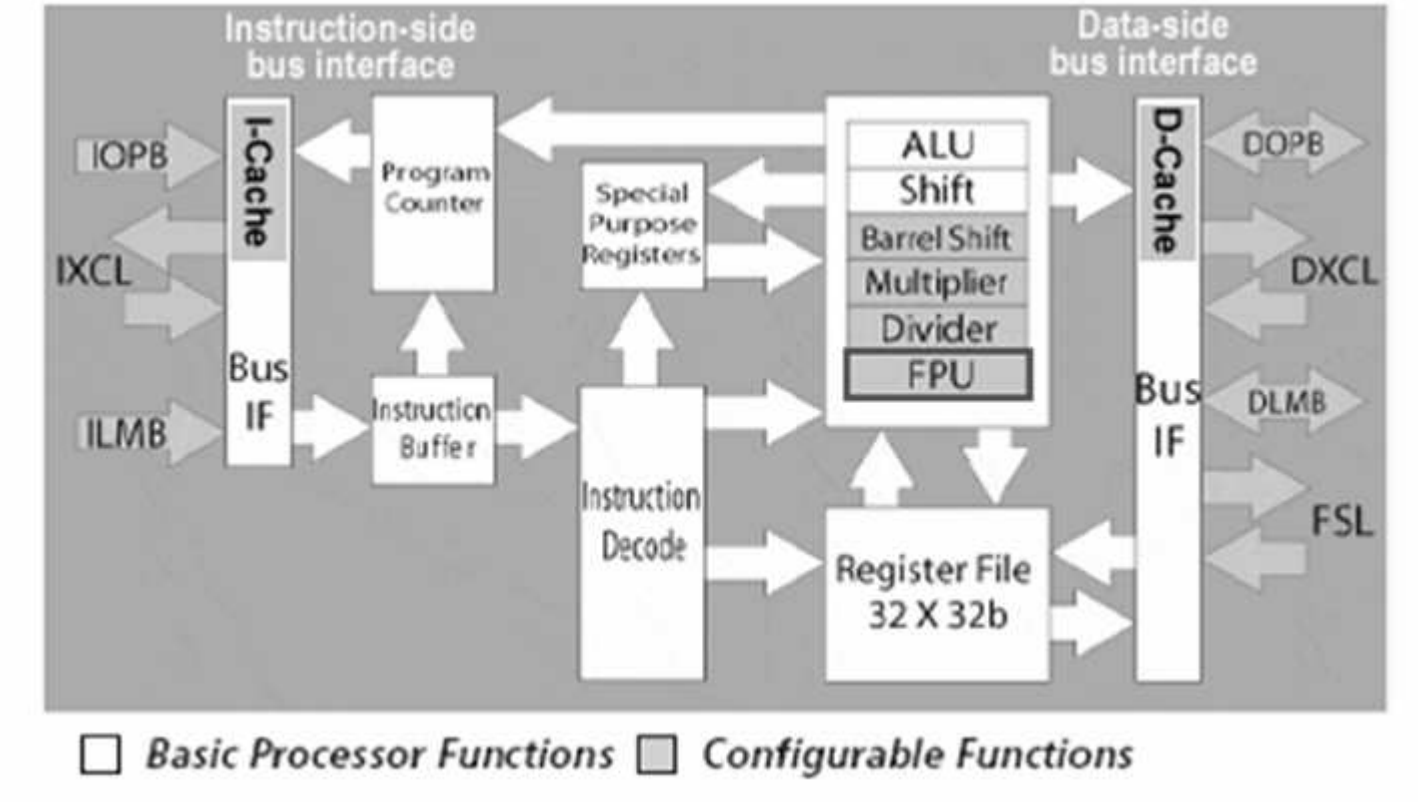
- Simulation
  - Speed: 500 MHz
  - Bandwidth Requested: 100 MB/s
- FPGA
  - Speed: 12.5 MHz, Max: 18 MHz
  - Bandwidth: 2.5 MB/s

DEMONSTRATION

Discussion Topics

- Which processor to use
  - SiHive: Moustique, General Purpose Core
    - Supports DTL: compatible with the network
    - Moustique takes about 20% LCs
  - Xilinx: Microblaze
    - Supports On-chip peripheral bus, FSL (Fast Simplex Link), Debug Interface
    - Takes about 2% LCs with a hard multiplier, barrel shifter and one FSL port

Microblaze Architecture



Discussion Topics

- Which board to use
  - SiHive Prototyping Board:
    - Can add upto 6 FPGA boards
    - Has a Peripheral Interface board with couple of USB's, Firewire, serial, parallel.
  - Celoxica:
    - Real applications can be better demonstrated
    - Lot of I/O options available: DVI, S-Video, Audio.