Farm of Streaming Engines (FaStE)

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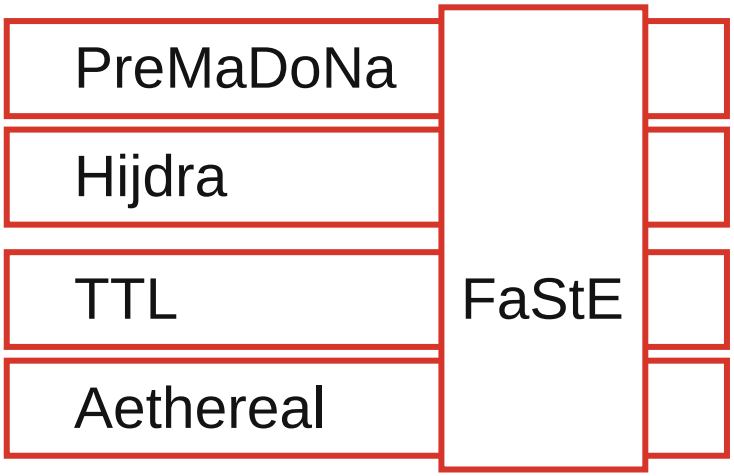
Digital Car Entertainment

Aim and context

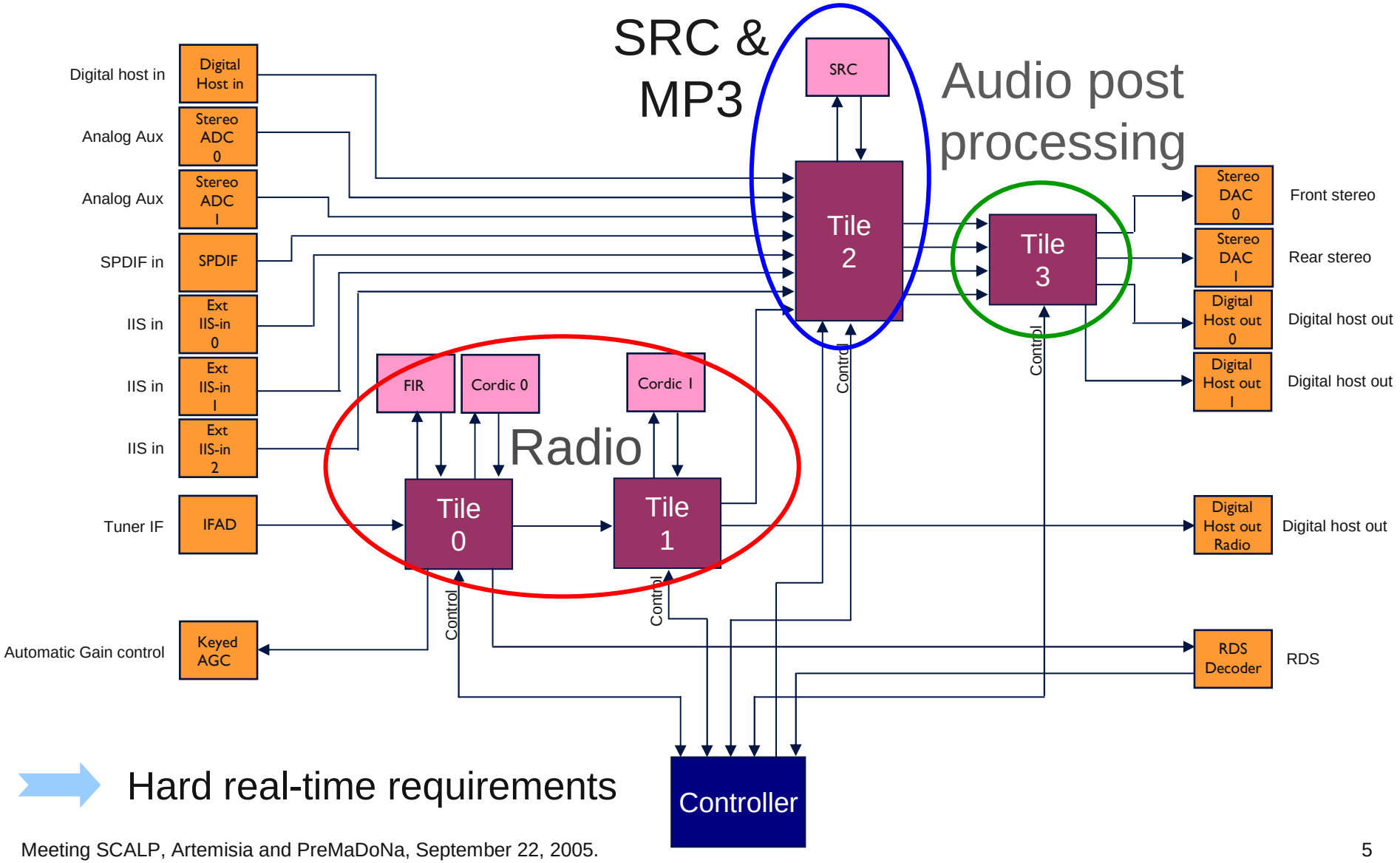
- Aim: to develop a multiprocessor for car infotainment where streaming and control are separated (a farm of streaming engines)
- The multiprocessor should support multiple streams/ applications (HRT/SRT)
- This implies an application driven approach (vertical slice) reusing the results of other methods driven projects (horizontal)



Overview

- In-car Digital Entertainment applications
- Architecture characteristics
- Exploration on the integration of a Aethereal network-on-chip (what is available today!)
- Proposed architecture for evaluation
- Future goals

Current In-car Digital Entertainment application



Hard real-time requirements

Applications next generations

Broadcast
- High Definition (HD) radio
- Satellite Digital Audio Radio Service (SDARS)

On demand audio service
- Ripping (e.g. encoding audio)

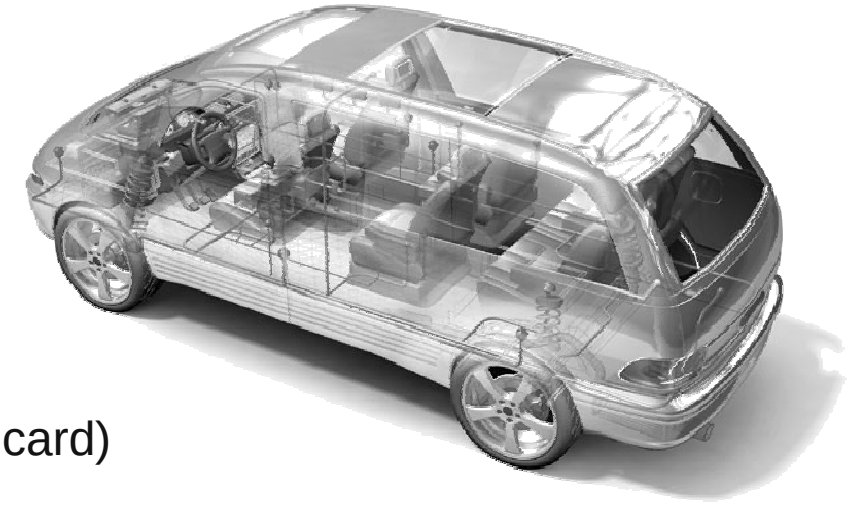
Audio quality (for car phone)
- Noise Reduction (NR)
- Acoustic Echo Cancellation (AEC)

Storage media
- CD/DVD
- Harddisk
- Removable discs (e.g. USB stick, flash card)

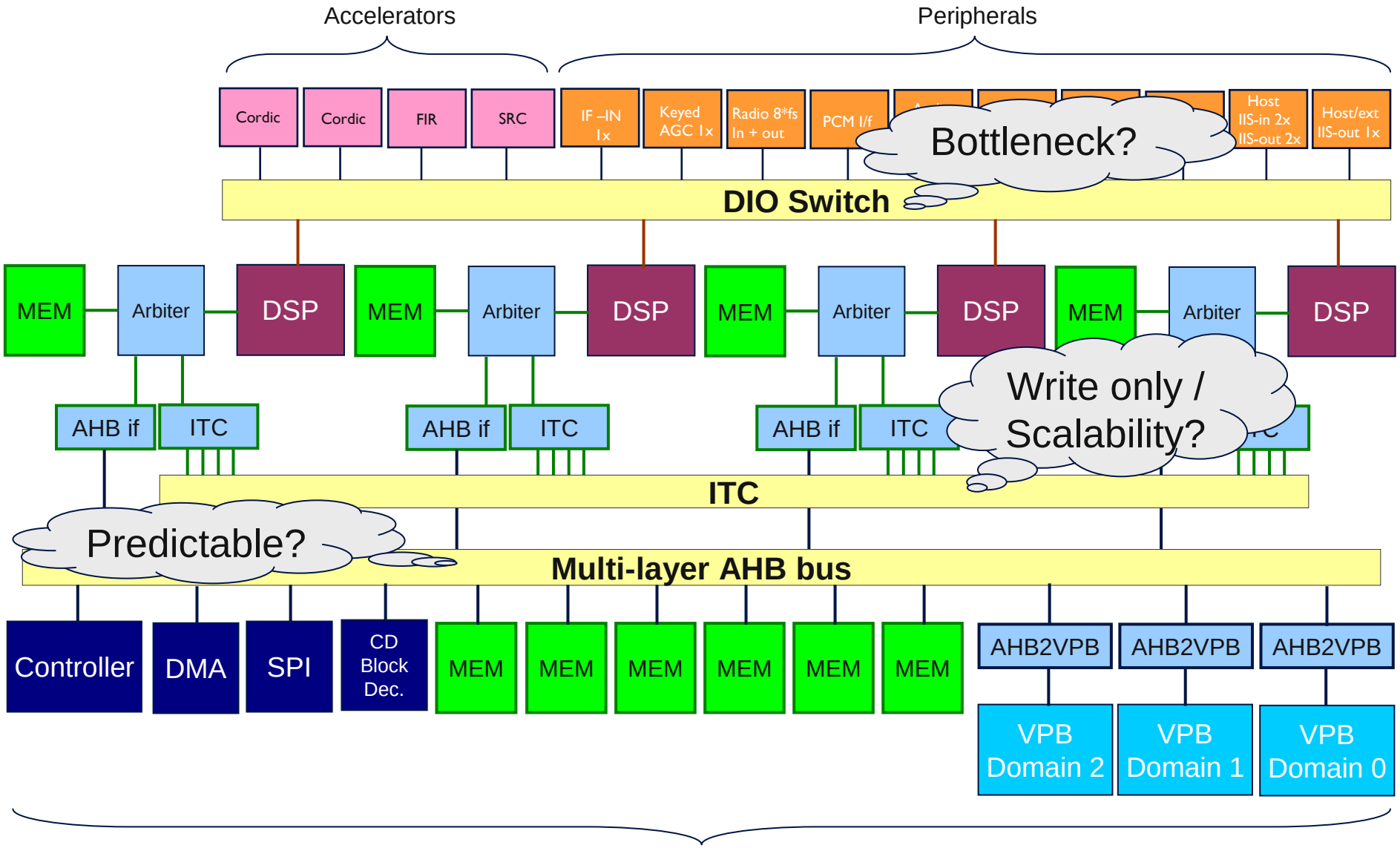
Connectivity
- Bluethooth
- USB
- WiFi

Navigation

Video



Current architecture characteristics



Expected resources for next generation

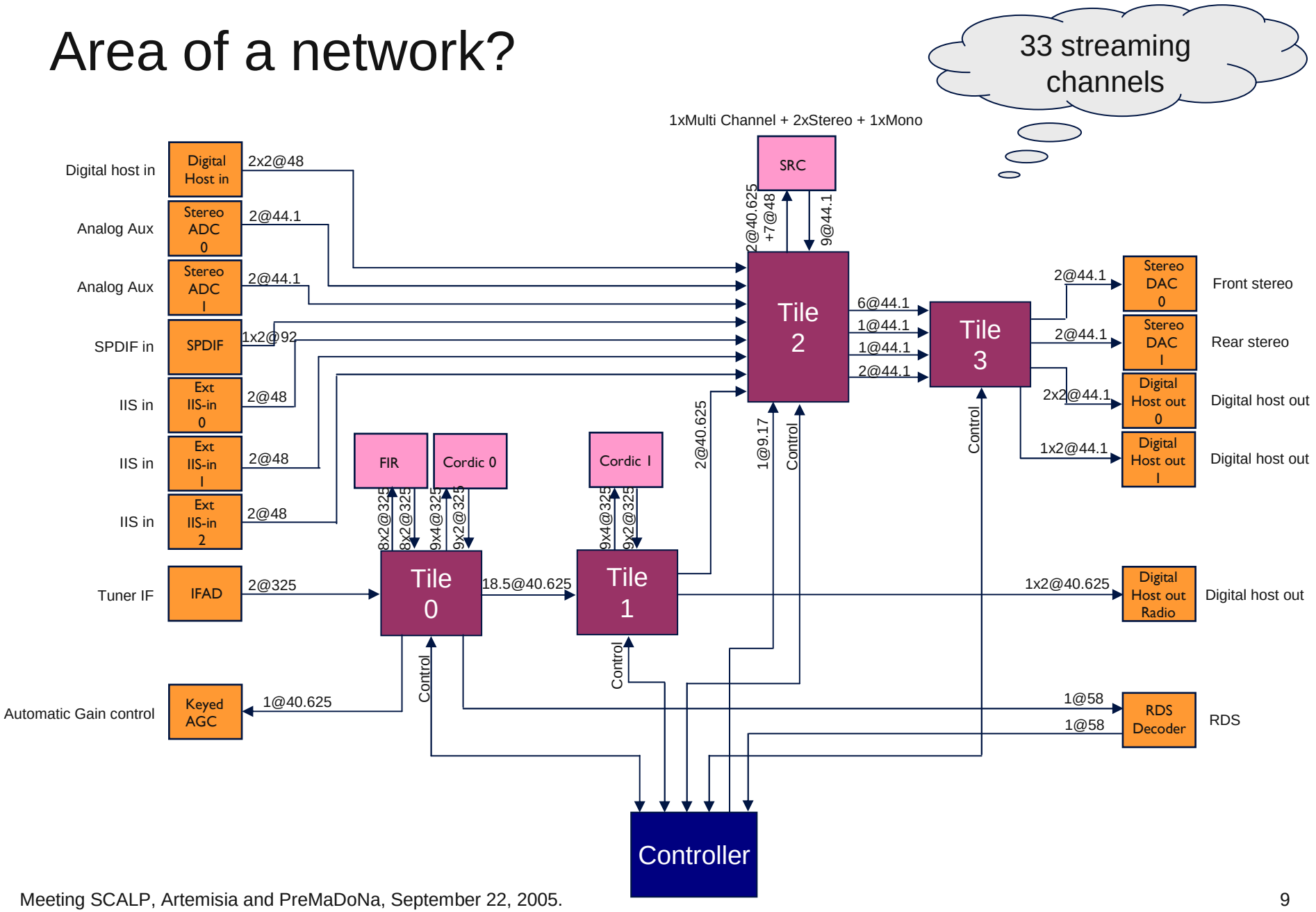
Viper
≈ 9M gates

	Generation			
	i	**i+1**	**i+2**	**i+3**
Technology	180 nm	90 nm	90 nm	65 nm
Power supply voltage core	1.8 V	1.5 V	1.5 V	1.2 V
Power supply voltage ana/IO	3.3 V	2.5 V	2.5 V	2.5 V
External connections	176	208	260	310
Number of gates	1,200,000 gates	2,700,000 gates	6,000,000 gates	13,000,000 gates
Number of flip flops	80,000 flip flops	180,000 flip flops	370,000 flip flops	800,000 flip flops
Frequency	130 MHz	195 MHz	300 MHz	430 MHz
Number of processors	5	8	12	17
Number of accelerators	3	6	9	12
Streaming processing power	545 MHz	1600 MHz	3000 MHz	6000 MHz

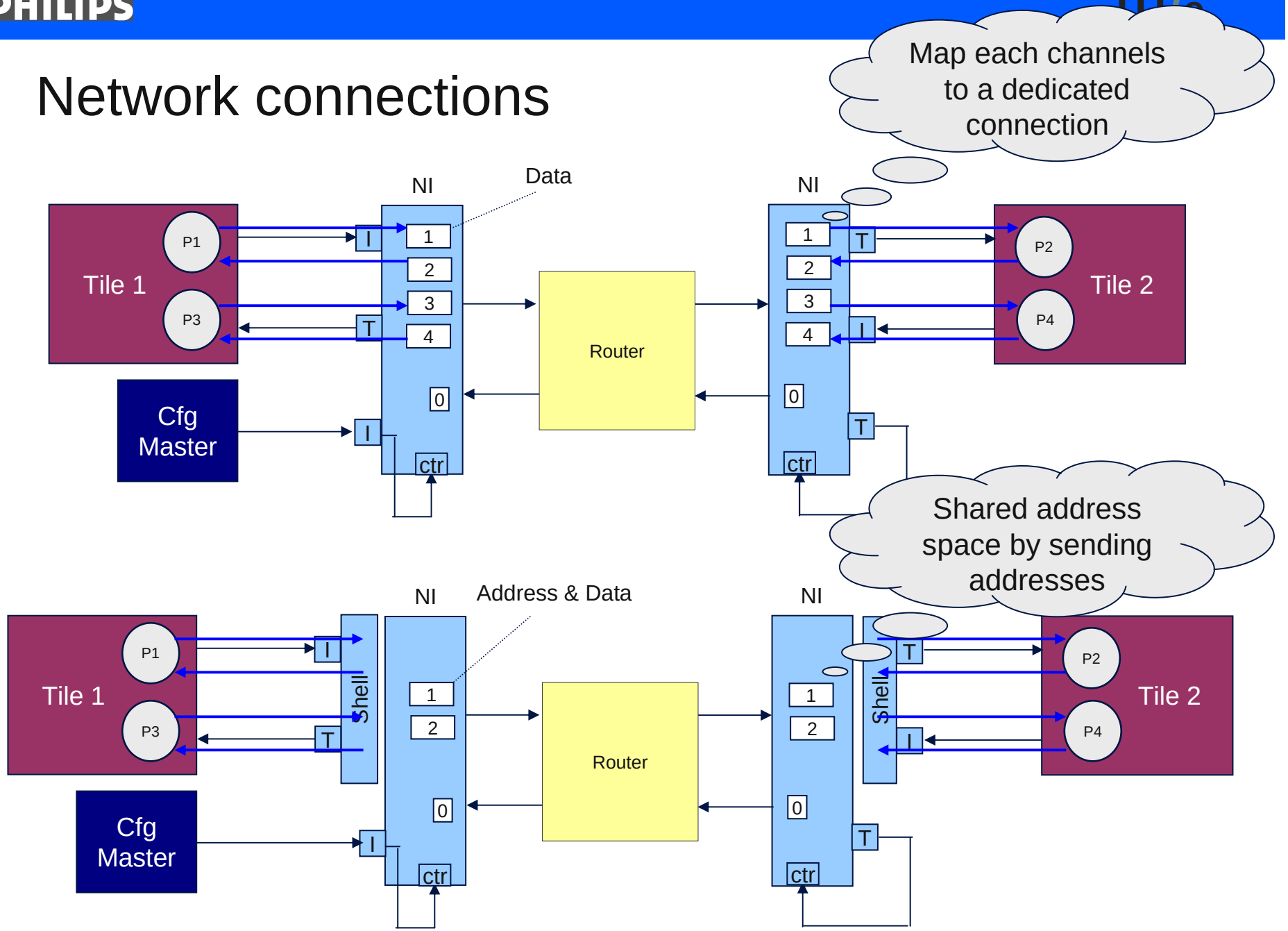
	Generation			
	i	**i+1**	**i+2**	**i+3**
DSP program memory	2,976 Kbit	8,200 Kbit	23,000 Kbit	63,000 Kbit
DSP data memory	948 Kbit	2,300 Kbit	6,700 Kbit	20,000 Kbit
DSP coefficient memory	420 Kbit	1,000 Kbit	2,800 Kbit	8,200 Kbit
Controller program memory	6,240 Kbit	x	x	x
Controller data memory	1,088 Kbit	x	x	x
Average memory per DSP tile	1,086 Kbit	1,643 Kbit	2,955 Kbit	5,365 Kbit
Memory content	55%	68%	77%	84%

DSP memory / (# processors–1)

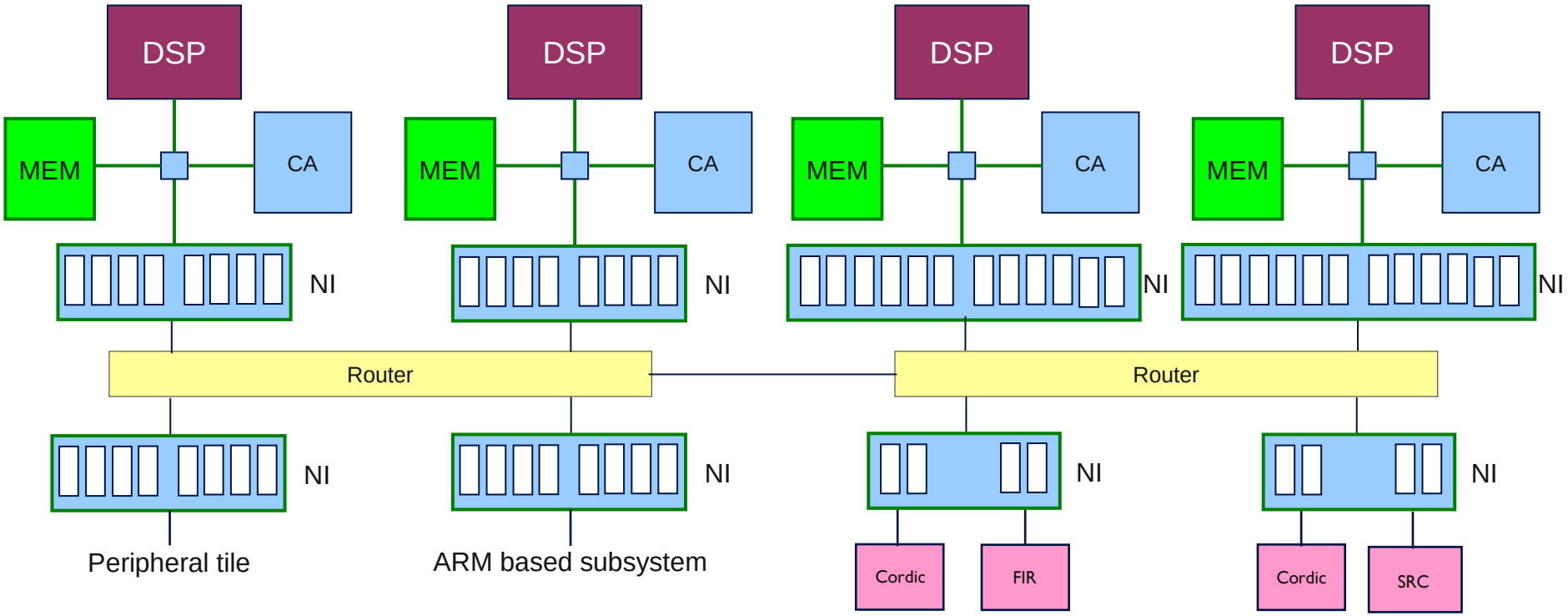
Area of a network?



Network connections



Proposed architecture for evaluation



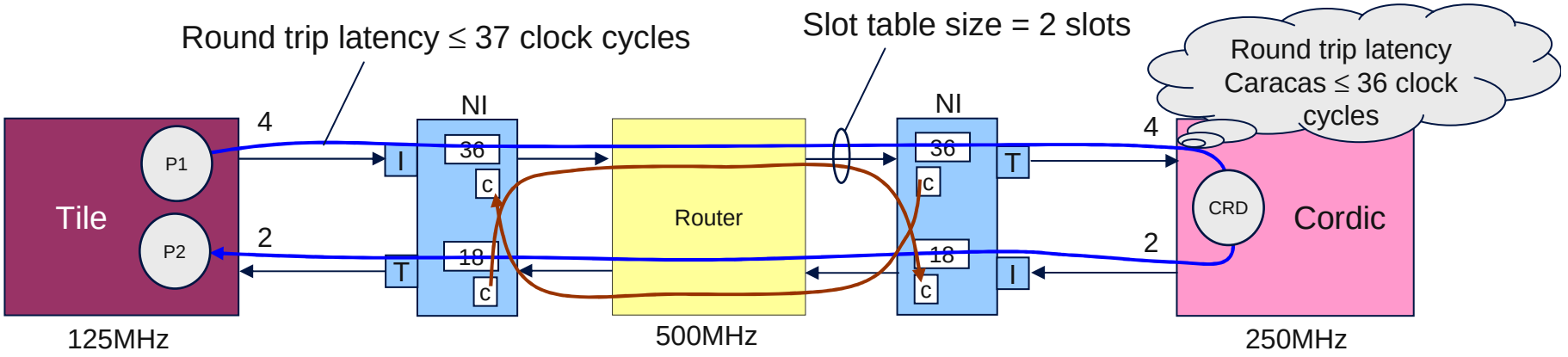
$$\text{Area}_{\text{interfaces}} = 0.734\text{mm}^2$$

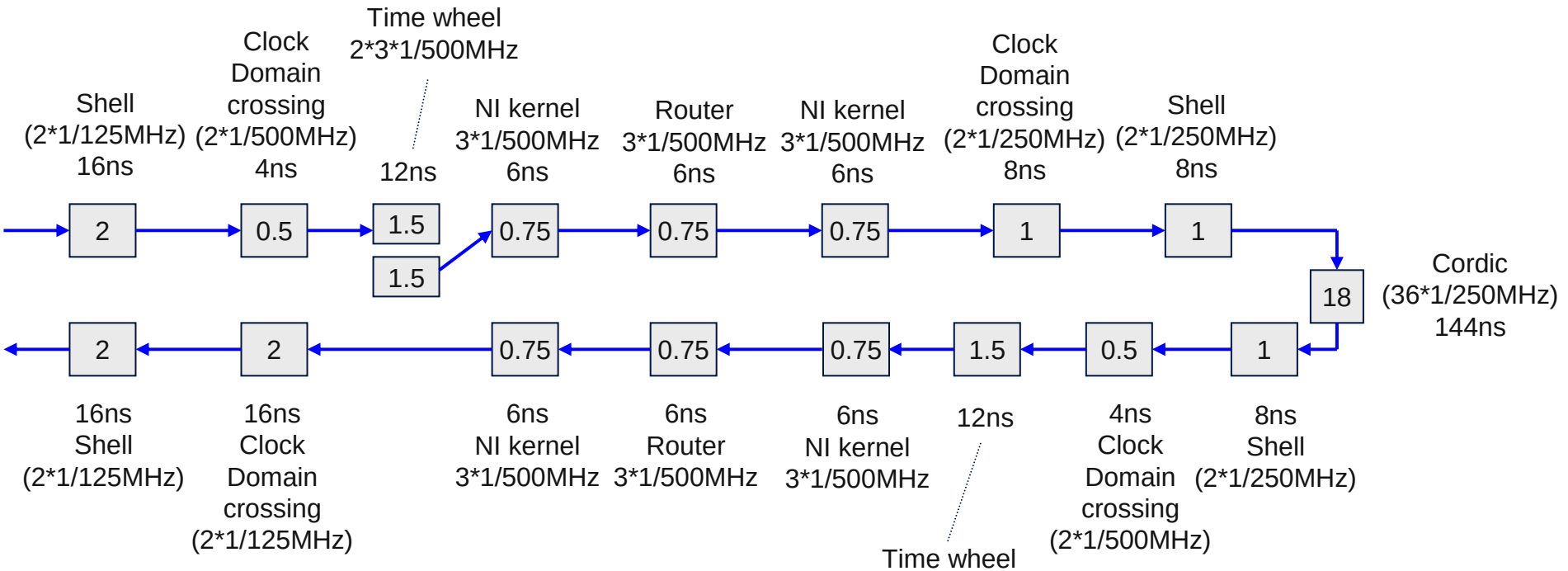
$$\text{Area}_{\text{routers}} = 0.270\text{mm}^2$$

$$\text{Area}_{\text{network}} = 0.734 + 0.270 = 1.004\text{mm}^2$$

Chip area increase
≈ 1.5%

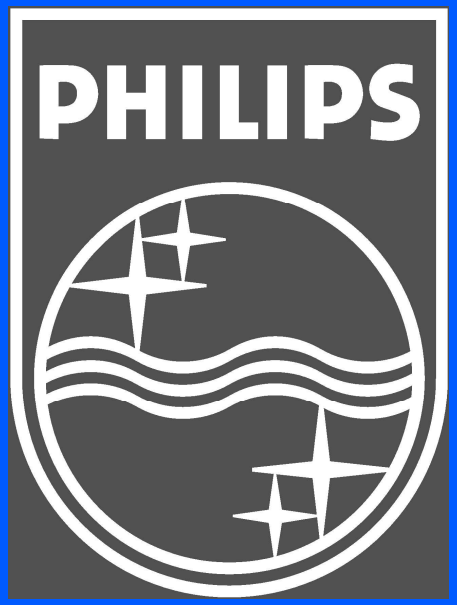
Latency of a GT connection





Future goals

- To build the proposed architecture in a **SystemC environment** using parts from Bolivar and Æthereal
- Have **models of the application and architecture** to derive the temporal behavior of the system
- **Mapping** applications to do **analysis** on the architecture and models
- **Definition of next generation** architectures for In-Car Digital Entertainment that support applications like audio, wireless streaming, connectivity, navigation, video, etc.



TU/e