THE AMD-K7™ PROCESSOR

Microprocessor Forum 1998

Dirk Meyer

AMD Processor Roadmap

Microprocessor Forum 1997

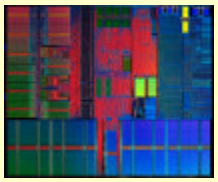
AMD

AMD-K7™

Performance

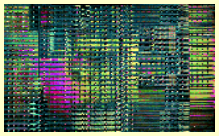
Sharptooth

µP Forum ‘98



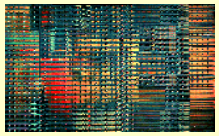
.25µ process
100 MHz Bus
On-chip, Full Speed Backside L2
100 MHz Frontside L3
Superscalar MMX Technology
3DNow! Technology

AMD-K6-2



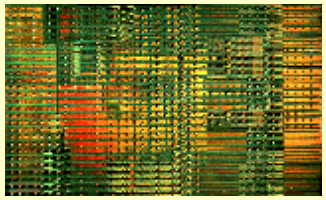
.25µ process
100 MHz Bus
100 MHz Frontside L2
Superscalar MMX Technology
3DNow!™ Technology

AMD-K6



.25µ process
Lower Power
Higher Speeds

AMD-K6®



.35µ process
MMX™ Technology
Enhanced

1H’97 **2H’97** **1H’98** **2H’98** **1H’99**

AMD-K7™ Processor Overview

AMD

- Superior 7th Generation CPU Design
- Leading Performance in Integer, Floating point, and Multimedia
- Operating Frequencies of 500 MHz+ using 0.25μm Technology
- High-speed Alpha™ EV6 Bus Technology
- High-speed Backside Level 2 Cache Controller
- Scalable Multiprocessing Architecture for Workstation and Server Markets
- Processor Module for Standard Motherboard Form Factors
- Optimized Chipsets, Motherboards and BIOS

AMD-K7™ Processor Architecture

AMD

- Three Parallel x86 Instruction Decoders
- 9-issue Superscalar Microarchitecture Optimized for High Frequency
- Dynamic Scheduling with Speculative, Out-of-Order Execution
- 2048-entry Branch Prediction Table & 12-entry Return Stack
- 3 Superscalar, Out-of-Order Integer Pipelines each Containing:
  - Integer Execution Unit
  - Address Generation Unit
- 3 Superscalar, Out-of-Order Multimedia Pipelines with 1-cycle throughput
  - FADD (4 cyc latency), MMX ALU (2 cyc latency), 3DNow!
  - FMUL (4 cyc latency), MMX ALU (includes Mul & MAC), 3DNow!
  - FSTORE
- Level 1 64K I-Cache & 64K D-Cache, each 2-way Set Associative
- Multi-level TLB (24/256-Entry I, 32/256-Entry D)

AMD-K7™ Processor Architecture (Con't)

AMD

- Two General Purpose 64-bit Load/Store Ports into D-Cache
  - 3-Cycle Load Latency
  - Multi-banking Allows Concurrent Access by 2 Load/Stores
- High-speed 64-bit Backside L2 Cache Controller
  - Supports Sizes of 512KB to 8MB
  - Programmable Interface Speeds
- High-speed 64-bit System Interface
  - First Mainstream Systems to have a 200MHz Bus
  - Significant Headroom for Future
- Deep Internal Buffering to Support Pipelines and External Interfaces
  - Up to 72 x86 instructions in-flight
  - 32 outstanding load misses
  - 15-entry integer scheduler
  - 36-entry floating point scheduler

Microarchitecture Terminology

AMD

- x86 Instructions are sent to one of two Decoding Pipelines:
  - DirectPath: Decodes common x86 instructions (1-15 byte lengths)
  - VectorPath: Decodes uncommon, complex x86 instructions
- Decoding Pipelines can dispatch 3 MacroOps to Execution Unit Schedulers
- Each MacroOp consists of one or two Operations (OPs)
- OPs are issued to the execution units

ADD	EAX, EBX	1 DirectPath MacroOp - 1 OP (ADD)
XOR	EAX, [EBX+8]	1 DirectPath MacroOp - 1 OP (LOAD) - 1 OP (XOR)
AND	[EBX], EAX	1 DirectPath MacroOp - 1 OP (LOAD/STORE) - 1 OP (AND)

Microarchitecture Pipeline

AMD

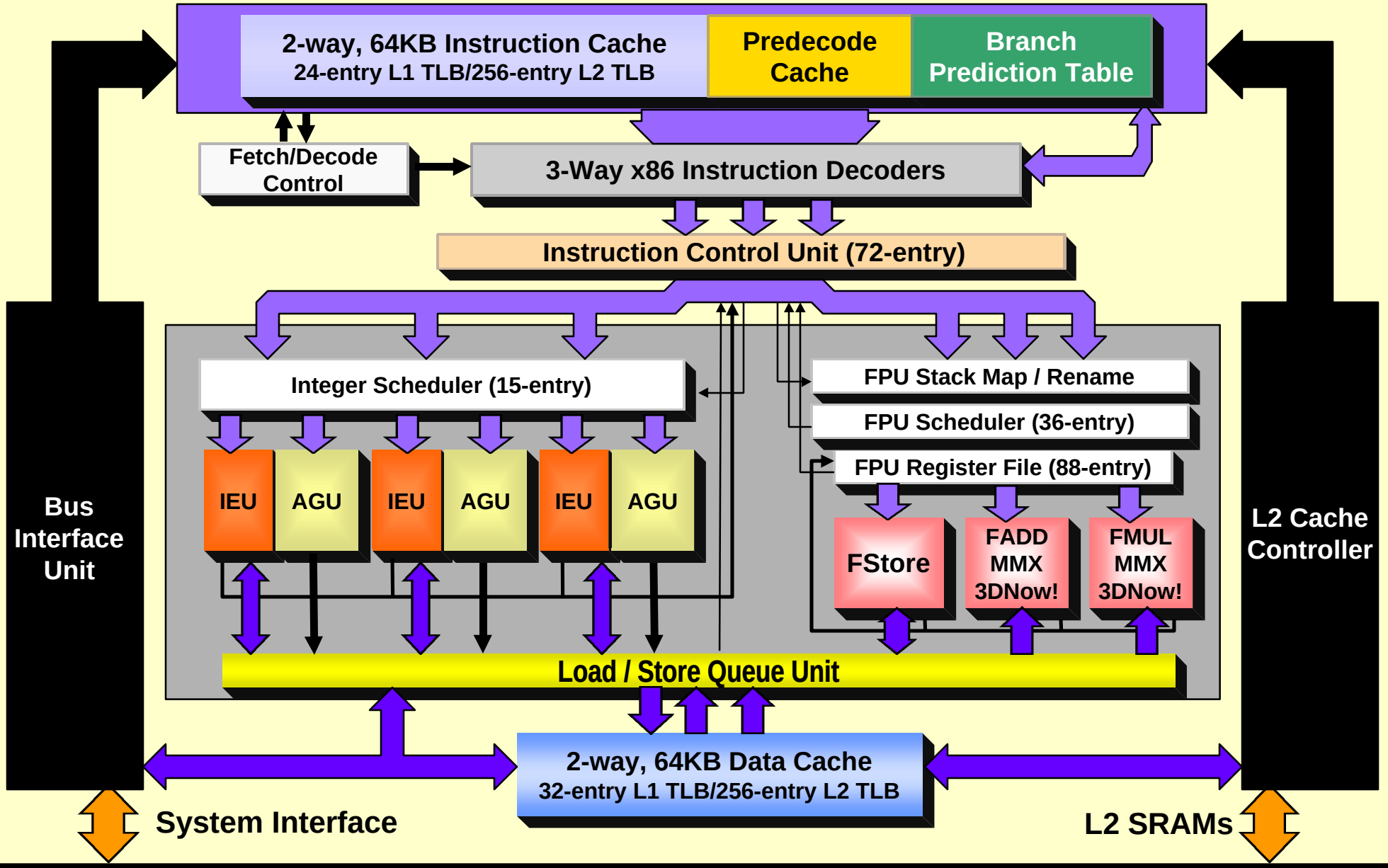
Integer Pipeline

1	2	3	4	5	6	7	8	9	10
Fetch	Scan	Align1	Align2 uRom	EDec	Idec Re-name	Sched	EX	Addr	DC

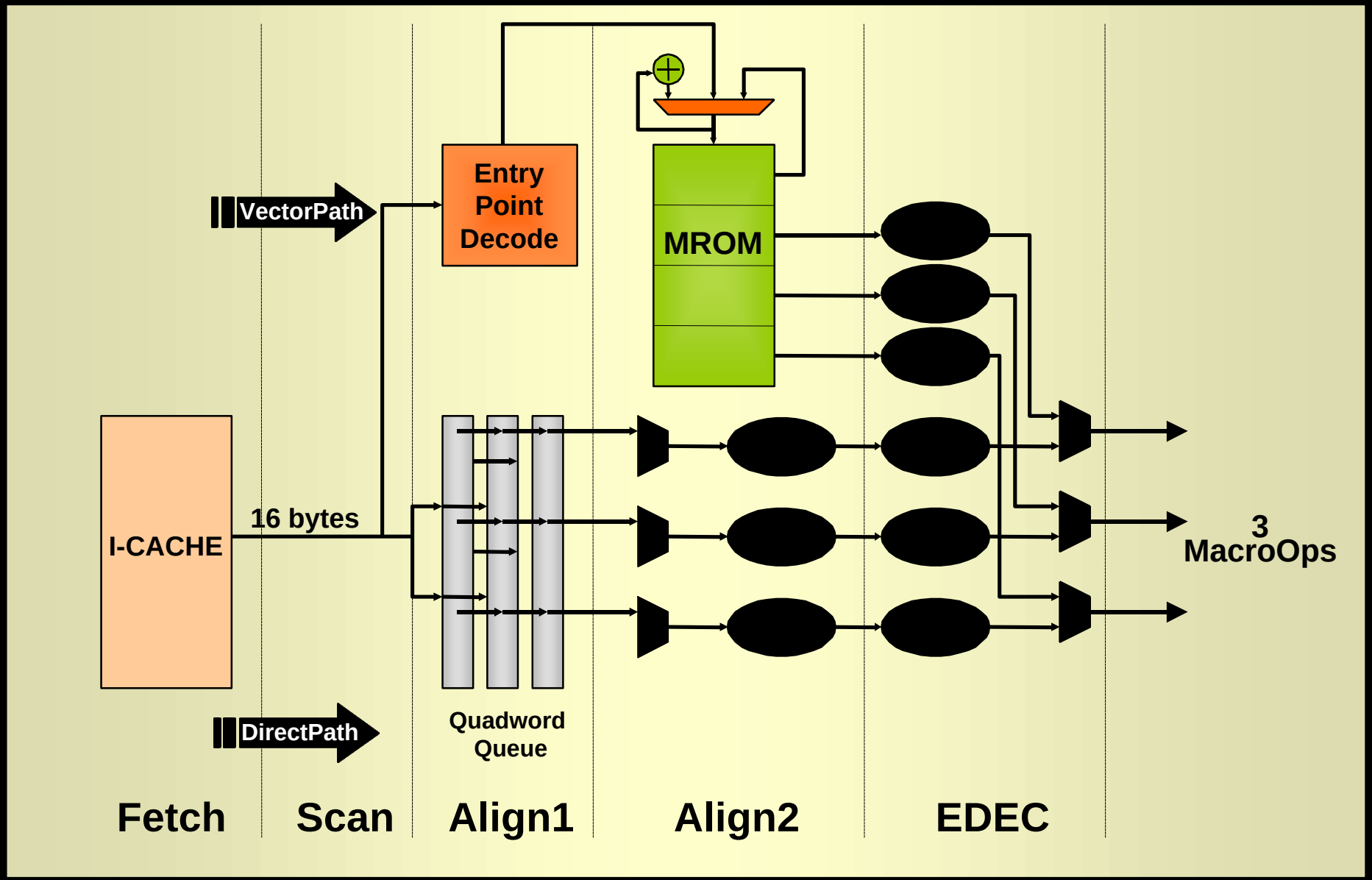
Floating Point Pipeline

7	8	9	10	11	12	13	14	15	
Stk Re-name	Reg Re-name	Wr. Sched	Sched	Freg	FX0	FX1	FX2	FX3	

AMD-K7™ Processor Block Diagram

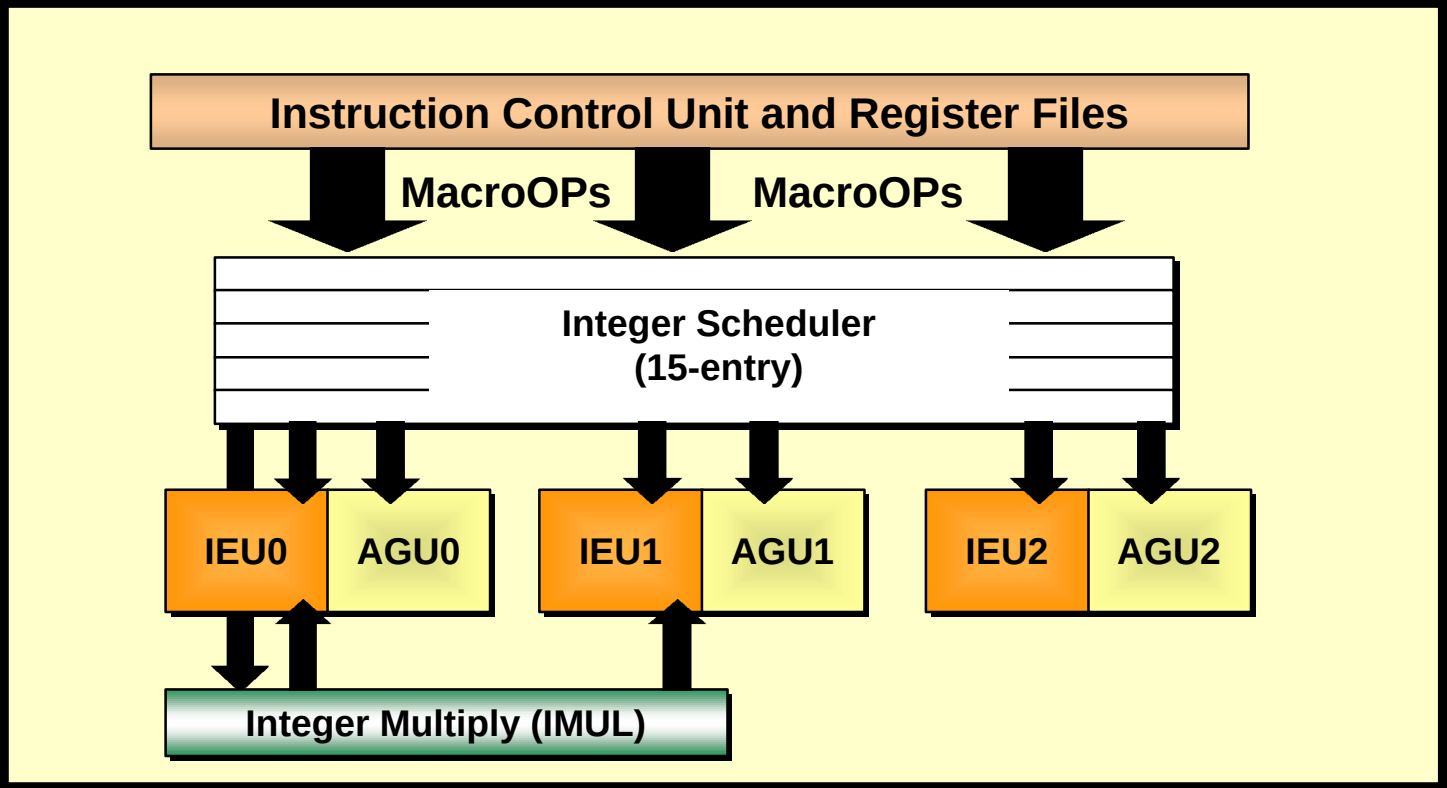


x86 Instruction Decoders



Integer Execution Units

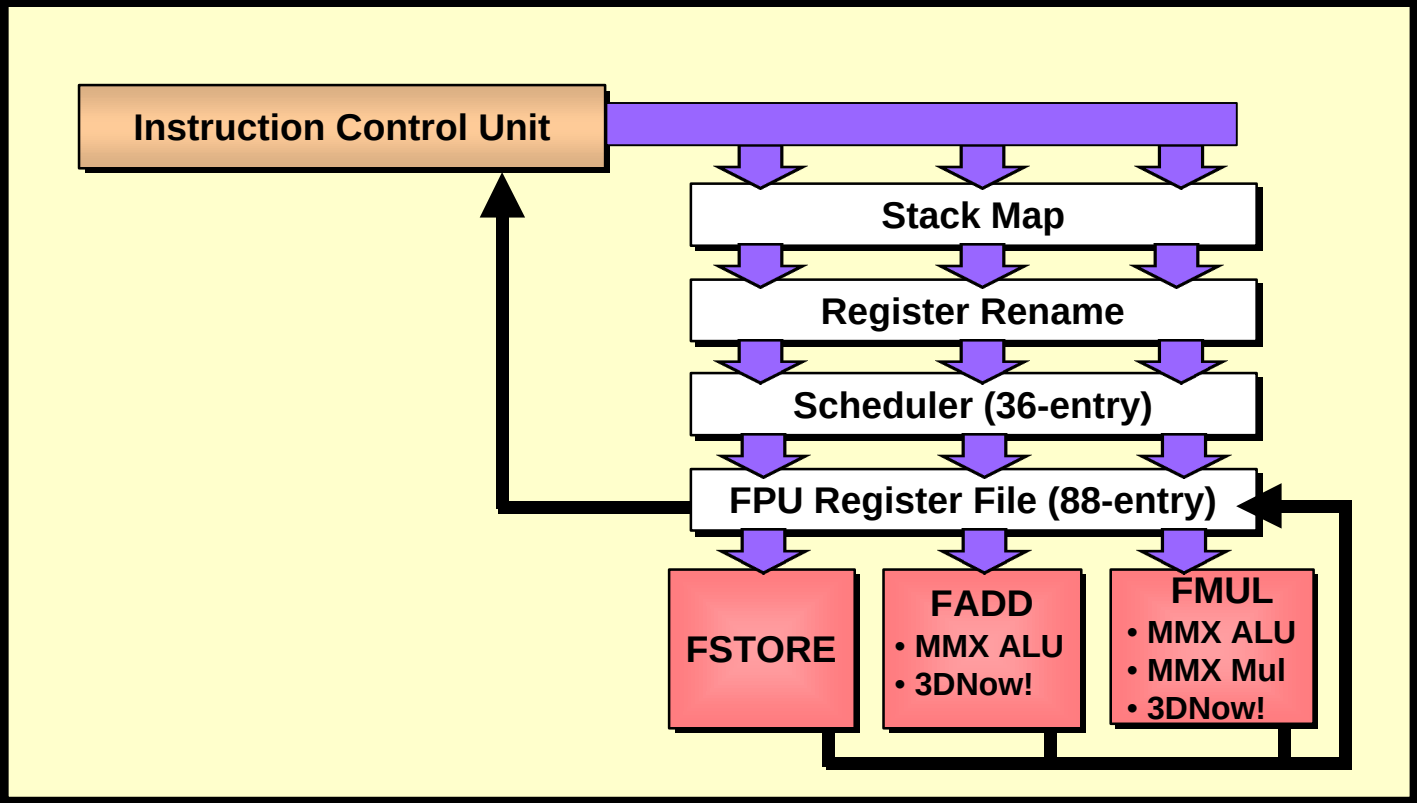
- Three Integer Execution Units (IEU)
- Three Address Generation Unit (AGU)
- 15-entry Integer Scheduler
- Full Out-of-Order Speculative Execution
- Multiplier



Superscalar Multimedia Execution Units

AMD

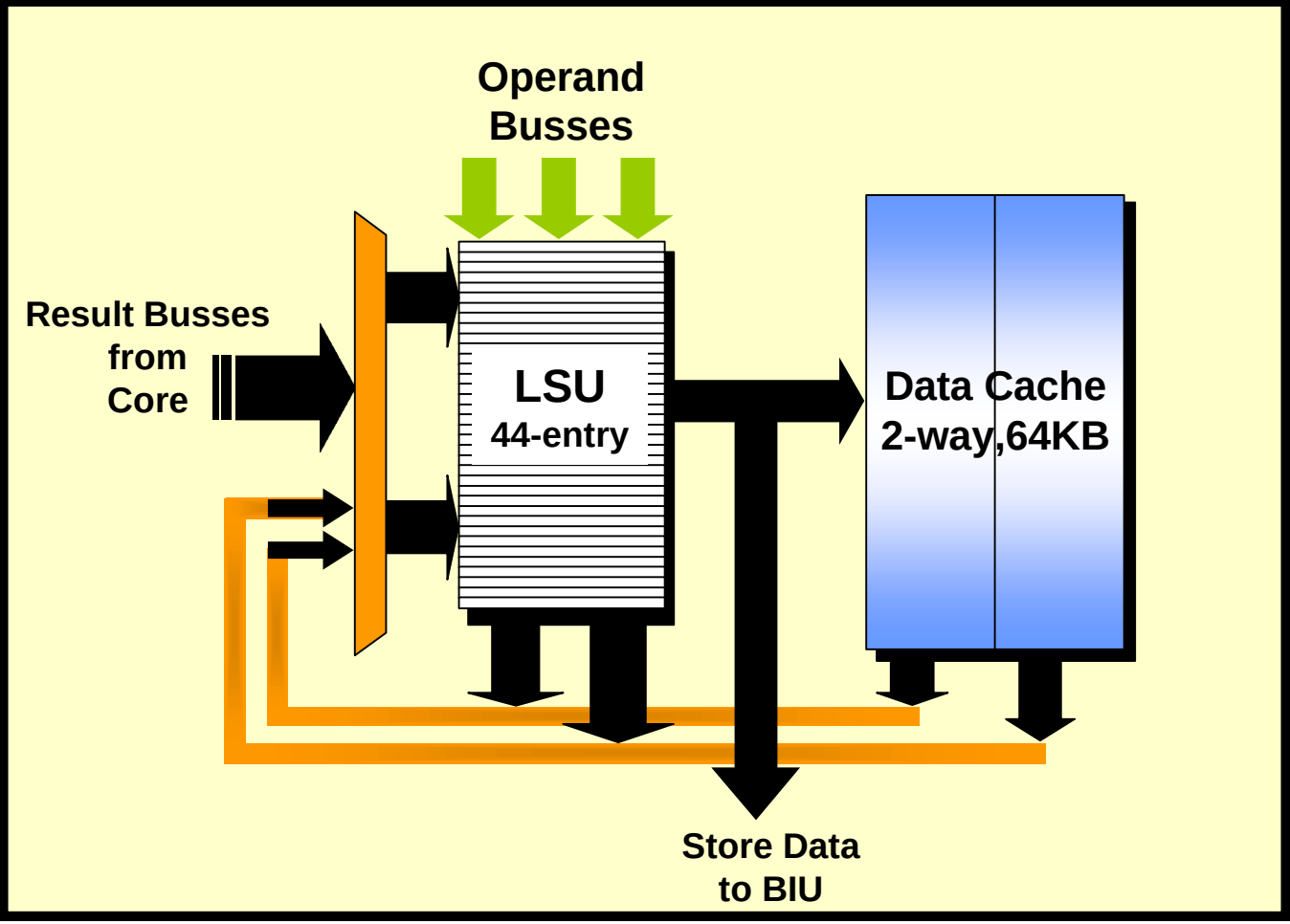
- Three Superscalar Multimedia Execution Units
- 3-issue, Out-of-Order, Fully Pipelined Design
- Separate Register File



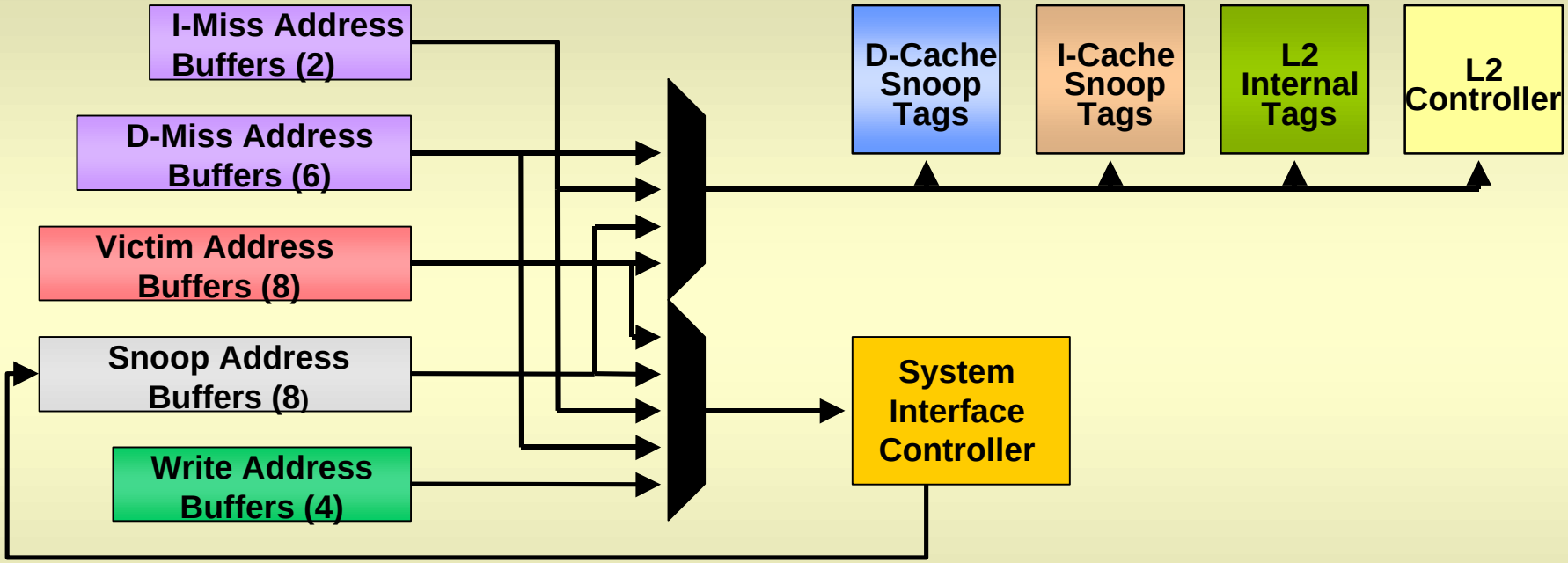
Load-Store Unit and Data Cache

AMD

- **Load Store Unit (LSU)**
  - 44-entry Load/Store queue
  - Data forwarding from stores to dependent loads
- **2-way, 64KB Dual-Ported Data Cache**
  - MOESI coherency, 64 byte line size
  - 32-entry L1 DTLB and 4-way, 256-entry L2 DTLB
  - 3 sets of data cache tags

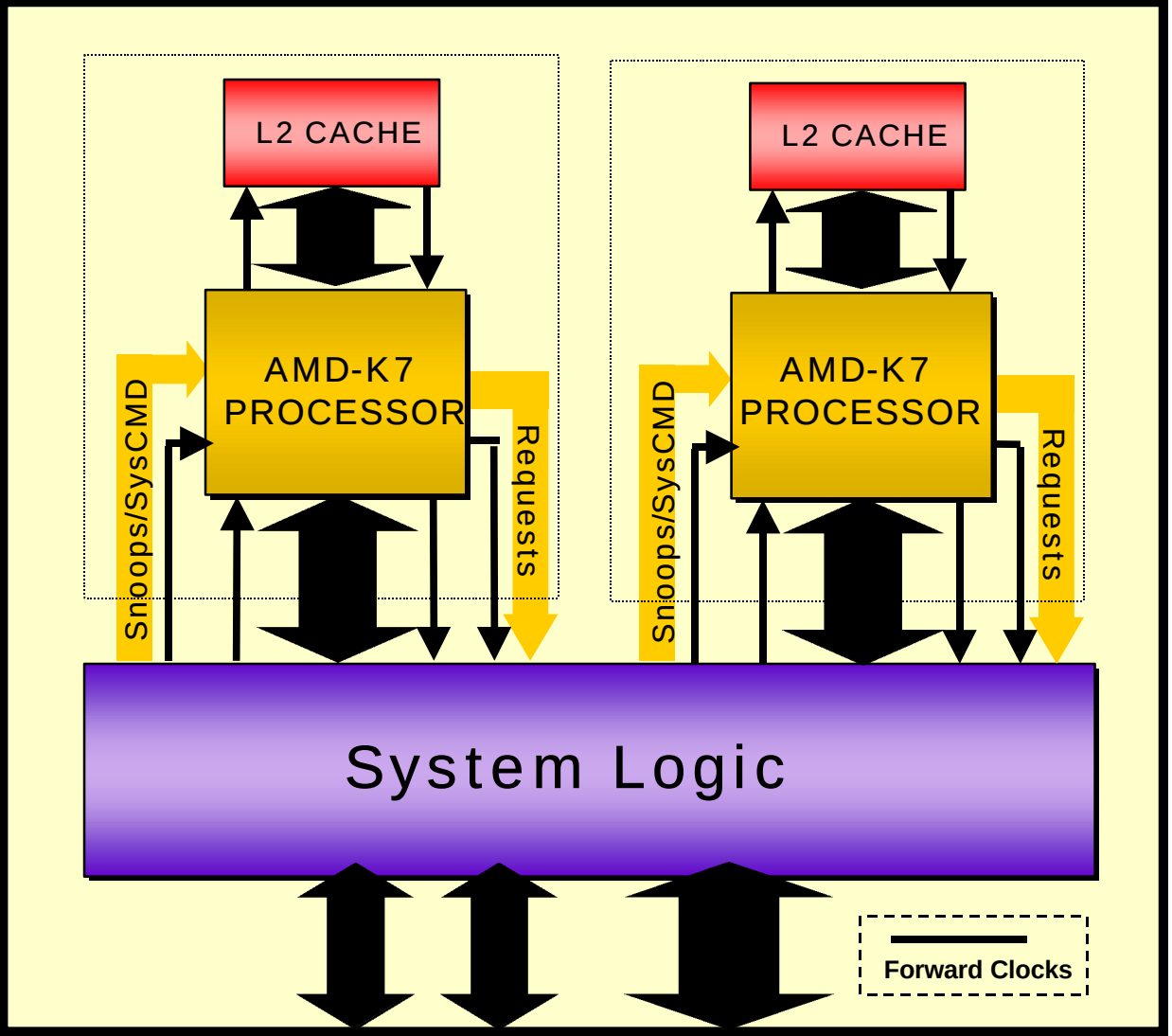


System Interface Controller Internals



System and L2 Cache Interfaces

- Alpha EV6 Bus Protocol
- Point-to-Point Topology with Clock Forwarding
- Decoupled Address and Data Busses
  - 72-bit Data Bus w/ ECC
  - Independent Address/Request Bus
  - Independent Snoop Bus
- Up to 20 Outstanding Transactions per Processor
- Scalable Multiprocessing
- L2 Cache Interface
  - 512KB to 8MB using Industry-Standard SRAMs
  - Programmable Interface Speeds
- Low-voltage Signaling



AMD-K7™ Processor Infrastructure

AMD

- **Chipsets**
  - Performance-optimized AMD-K7 chipsets are planned from both AMD and leading third-party vendors in 1999
- **Motherboards**
  - High quality, performance-optimized AMD-K7 motherboards are planned from leading vendors at launch in 1H99
- **BIOS**
  - Production BIOS are planned from all leading suppliers including AMI, Award and Phoenix
- **Mechanical**
  - The AMD-K7 processor will utilize existing industry-standard physical/mechanical infrastructure components including cases, power supplies, fans, heat sinks, etc.

AMD-K7™ Processor Summary

AMD

- **Superior 7th Generation Processor Architecture**
  - Advanced Processor Core Design
  - Leading Edge Frequencies: 500MHz+ using 0.25µm Technology
  - High Performance System Interface with low-voltage swing Point-to-Point Topology and Clock Forwarding Technology
  - Scalable Multiprocessing Architecture
- **AMD-K7 Processor Module, Chipsets, Motherboards**
- **Leading Edge Silicon Technology**
- **Fab 25 and Fab 30 Provide Volume Production Capacity**