Abstract – Advanced technology nodes employ a large number of innovations. In addition, they require ‘scaling boosters’ in the design of standard-cell libraries to be able to offer the scaling benefits in area, performance, and power that we have grown accustomed to. Consequently, sub-10nm standard cells are significantly more complex than their predecessors.

Cell-aware test (CAT) explicitly targets cell-internal resistive open and short defects identified through extensive characterization of the library cells. This paper is (to the best of our knowledge) the first to report on the application of CAT library characterization on a sub-10nm technology node. We used Cadence’s CAT tool flow on an experimental 114-cell library in IMEC’s 3nm CMOS technology iN5. Despite the increased cell complexity, we show that the CAT flow still works, and that compared with functionally-comparable library cells in a 45nm technology, the number of potential non-equivalent defect locations, cell-level test patterns, and defect coverage did not change drastically.

1 Introduction

Driven by a seemingly unsatisfiable hunger for ever more compute power, the semiconductor industry has in the last two decades gone through technology nodes of (1997) 0.35µm, 0.25µm, 0.18µm, 0.13µm, 90nm, 65nm, 45nm, 28nm, 22nm, 14nm, and 10nm (today) [1]. Originally, node names referred to the transistor gate length, and later to the half-pitch of the bottom metal interconnect layer (‘Metal-1’). However, since the 22nm node, the link between node name and minimum feature size has been lost, and today node names are merely marketing names for subsequent technology generations; equal node names for technologies from different manufacturers do not necessarily have the same feature sizes.

The traditional scaling strategy, based on decreasing minimum metal pitch (MMP) and contacted poly pitch (CPP) alone, does no longer provide sufficient performance benefits for nodes below 10nm [2]. Hence, designers of standard-cell libraries have now also become directly involved in the scaling rat race. They implement innovative library-cell design concepts (referred to as scaling boosters) that provide additional area, performance, and power benefits. The combined benefits of technology and cell-design scaling obtain chip area reductions of ~40%, which allows us to (more-or-less) maintain Moore’s Law [1], but more importantly to justify the financial investments required to transition to the next technology node [3].

Cell-aware test (CAT) explicitly targets defects inside library cells and therefore significantly reduces the amount of test escapes compared to conventional automatic test pattern generation (ATPG) approaches that cover cell-internal defects only serendipitously. CAT has demonstrated its value in effectively reducing test escape rates on numerous technology nodes already: 130nm [4], 90nm [5], 65nm [5, 6], 45nm [7], 32nm [8], and 14nm [9]. All these technology nodes utilize planar FETs, apart from the 14nm node, which is based on FinFETs.

In this paper, we describe several of the technology and cell-design innovations that are encountered in advanced sub-10nm nodes. As a vehicle we use imec’s iN5 standard-cell library (which corresponds to what commercial foundries would refer to as a ‘3nm’ CMOS node). We perform library-cell defect characterization with Cadence’s CAT tool flow on the iN5 library cells. To the best of our knowledge, this paper is the first to report CAT results for a sub-10nm standard-cell library.

Our CAT results are comprised of (1) defect-location identification (DLI) [7] on the basis of parasitic extraction, (2) defect characterization on the basis of detailed accurate analog simulations of library cells and their potential defects, and (3) defect-detection matrix (DDM) manipulations [10] to optimize downstream cell-aware ATPG results on circuit designs based on the iN5 standard-cell library. The results demonstrate that, despite the increased complexity in the library-cell architecture, our CAT tool flow still works and the number of potential open- and short-defects which need to be simulated for characterization and later to be covered by cell-aware ATPG is very similar to mature technologies.

The remainder of this paper is organized as follows. IMEC’s iN5 technology node and corresponding standard-cell library are de-
telled in Section 2. Section 3 describes Cadence’s CAT flow we use to characterize the iN5 library cells. Experimental results are presented in Section 4, while Section 5 compares those to results on comparable cells in Cadence’s GDPK045 library in 45nm CMOS. Section 6 concludes this paper.

2 iN5 Standard-Cell Library

Research institute IMEC explores the various technology-node scaling directions for and with the semiconductor industry. Engineering teams from IMEC and its partners couple theoretical research to practical implementation in IMEC’s state-of-the-art IC manufacturing facilities. In that context, IMEC has developed experimental process technology nodes and corresponding standard-cell libraries that are named iN8, iN7, and iN5 and correspond to what commercial foundries would refer to as respectively ‘7nm’, ‘5nm’, and ‘3nm’ CMOS nodes. In this section, we describe the scaling path from iN7 to the most advanced of these nodes, viz. iN5, as well as several technology and design features of iN5. Feasibility of the iN5 technology and standard-cell library have been demonstrated in a joint IMEC-Cadence test-chip of a 64-bit microprocessor, for which the tape-out was reported in 2018 [11].

The area of a library cell is determined by the product of its height and its width. The height is the product of MMP and the number of metal tracks; for standard cells, this implies that both MMP and track count are fixed throughout the entire library. The width of the standard cells is the product of CPP and the number of poly lines; the latter is determined by the complexity of the logic function that the cell implements. Traditionally, the transition from one technology node to the next was effectuated by scaling both MMP and CPP with a factor 0.7, which resulted for the same function in $0.7 \times 0.7 = 49\%$ of the original area.

For sub-10nm nodes, scaling MMP and CPP only does not bring sufficient performance benefits any more. IMEC coined the term design/technology co-optimization (DTCO) to indicate the involvement of library-cell designers to maintain sufficient area, performance, and power benefits for scaling below 10nm [12, 13]. An effective strategy for some of the node transitions is to reduce the number of tracks of the first metal layer, in addition to pitch scaling [14]. Track scaling was employed in the definition of IMEC’s 7nm, 5nm, and 3nm technology nodes. In the meantime, to support routability within cells, an extra intra-cell metal layer has been introduced: MINT. MINT is the first metal layer and consequently Metal-1 becomes the second metal layer. In mature nodes, only one metal layer, Metal-1, was used for cell-internal interconnections and power rails. Metal wires in older technology nodes could be routed with 90° bends in the $xy$ plane. For performance and financial reasons [13, 15], such bends are no longer permitted in IMEC’s sub-10nm technologies; MINT and Metal-1 wires run exclusively in the $x$ respectively $y$ axis direction.

Even though from the 45nm technology onwards, the gate material was changed from polysilicon to metal, the term ‘poly’ is still kept as gate, hence CPP is metal gate pitch for iN5 technology. Figure 1 shows in conceptual drawings the scaling steps from IMEC’s iN7 (‘5nm’) to iN5 (‘3nm’) nodes, with iN6 as an intermediate (‘half’) node [3]. In the step from iN7 to iN6, MMP is scaled with 25% from 28nm down to 21nm. CPP scaling is only with a meagre 6.25% from 48nm down to 45nm, as the overall industry trend is that poly pitch scaling slows down due to difficulties to keep pace with device performance and yield issues. Along with scaling the number of metal tracks from 6.5 down to six, a total area reduction of 35% is achieved. To reach the iN5 node, further scaling MMP and CPP is not feasible [3], and therefore, the iN5 area benefits are due to an additional height reduction down to five metal tracks. However, with two metal tracks dedicated to power and ground rails, the three remaining metal tracks would be too few to allow sufficient routability freedom inside the cells. Therefore, it was decided to move the power rails to a level below the device layer; so-called buried power rails (BPRs) [16]. This frees up the necessary space in a five-track standard cell height for four metal tracks as cell-internal routing resources. As Figure 1 shows, the five-track cell height also forced us to drop one of the two fins per transistor. From iN6 to iN5, an additional 17% area reduction is achieved, making the area benefits step from node iN7 to iN5 $(1 - 0.35) \times (1 - 0.17) = 54\%$, well above the required minimum scaling target of 40%.

Figure 2 shows as example the inverter cell INVD1 from the iN5 library. Figure 2(a) shows the top-view layout and Figure 2(b) depicts a three-dimensional model of the cell. In the iN5 technology, the layer sequence, from bottom to top, is BPR, the device layer, MINT, and Metal-1. The device layer contains fin, metal gate, and M0A. M0A provides contacts to fins, acting as source or drain of the FinFET transistors.

The rule that MINT wires can only be routed in horizontal direction impacts gate-contact locations. As all gate contacts go to the MINT layer, it is impossible to arrange the interconnections to the MINT layer on one line, as shown in Figure 3(a). A solution is shown in Figure 3(b). Gate contacts are shifted up and down for two neighboring gate bars, respectively. As the fin count is reduced to one,
the contact area on M0A depends on the overlay area between the MINT wire and M0A. Due to patterning limitations, we use a single contact on the maximum overlay area. In a planar technology, parallel contacts from metal to a diffusion well are used to increase manufacturing yield.

![Image](image_url)

**Figure 3:** Moving gate contacts from (a) the center to (b) the extremes of the gate lines.

In the iN5 technology, CPP = 45nm and Metal-1 pitch = 30nm; this is a ratio of 3:2. This implies that between every two gate pitches, we can fit three Metal-1 pitches, see Figure 4(a). Consequently, if a cell of which poly and metal lines ending with the relative location shown in Figures 4(b) is placed in a row, the next cell’s poly and metal lines should start with the relative location shown in 4(c), and vice versa, to prevent Metal-1 being off-grid at circuit level. Therefore, two versions of relative locations between poly and metal-1 lines are designed for each library cell in the iN5 technology.

![Image](image_url)

**Figure 4:** Three Metal-1 pitches and two gate pitches between every 90nm leads to two versions of Metal-1 routing between every two gate lines.

## 3 Cell-Aware Test

The Cadence CAT tool flow is depicted in Figure 5 [7, 10]. It consists of three steps: (1) defect-location identification (DLI) [7], (2) defect characterization, and (3) cell-aware ATPG. The first two steps are executed once per cell-library version, while the last step is specific to a particular IC design. The interface between Steps 1 and 2 on the one, and Step 3 on the other hand is formed by a set of defect-detection matrices (DDMs), one per library cell. DDMs are binary matrices in which we encode which cell-internal defects of defect-detection matrices (DDMs), one per library cell. DDMs are binary matrices in which we encode which cell-internal defects are detected by which cell-patterns are binary matrices in which we encode which cell-internal defects of defect-detection matrices (DDMs), one per library cell. DDMs are binary matrices in which we encode which cell-internal defects are detected by which cell-patterns are binary matrices in which we encode which cell-internal defects of defect-detection matrices (DDMs), one per library cell. DDMs are binary matrices in which we encode which cell-internal defects are detected by which cell-patterns are binary matrices in which we encode which cell-internal defects are detected by which cell-patterns.

Step 1, defect-location identification [7], determines both a full set as well as a compact set of defect locations. The full set contains all potential locations of both open and short defects for intra-cell interconnections and transistors. Defects potentially happening on and between cell-internal interconnections are identified based on layout analysis implemented by Cadence’s parasitic extraction (PEX) tool Quantus™. Transistor-internal defects are modeled as opens on and shorts between transistor terminals. By default, opens on gate, source, and drain terminals are modeled for each transistor; a short is identified between each terminal pair of gate-source, gate-drain, source-drain, and gate-bulk. The DLI function in Cadence’s ATPG tool Modus™ creates a compact set of defect locations out of the full set by selecting one representative defect location for each set of defects with equivalent fault effects. This compact set with defect locations is typically significantly smaller than its corresponding full set; [7] reported a reduction of 97.2%. This reduction translates itself into a proportional reduction of simulation time in Step 2, without loss of test quality. The full set of defect locations is stored for later use during failure analysis.

Step 2, defect characterization, is a function in Modus. It adds a resistive value to the defect locations; this allows us to model hard as well as weak resistive open- and short-defects. The defects and the defect-free netlist are submitted to the Transient Fault Analysis function of Cadence’s analog simulator Spectre® [17]. For a given defect d and cell-pattern p, if and only if the simulation of corresponding defect-free and defective netlists result in a different cell output value, p is capable of detecting defect d. The detection data is stored in a DDM per cell.

We have developed two algorithms, which subsequently manipulate the DDMs in order to optimize the downstream ATPG results with respect to fault coverage, chip-level test pattern count, and ATPG compute time [10]. A first algorithm extends DDMs with fully-specified patterns only to include also all applicable partly-specified patterns. During cell-to-chip expansion, the ATPG tool now has a possibility to select test patterns with only necessary care bits. This increases fault coverage and reduces test-pattern count. A second algorithm selects, for a given DDM, the subset of patterns that (1) provide full defect coverage and (2) minimizes their total care-bit sum. We exploit these preferential patterns in Step 3.

Step 3, cell-aware ATPG, uses DDM cell-patterns as starting point for chip-level test pattern generation. It tries to maximize the coverage of the detectable cell-internal defects for the DDM of the cell type, while minimizing the number of chip patterns. Forcing ATPG to first try to expand these preferential patterns keeps the ATPG compute time under control.

## 4 Cell-Aware Test on iN5 Cells

In this section, we provide experimental results of DLI, defect characterization, and DDM optimization of all iN5 cells. The used tools versions are Modus v19.1, Quantus v18.1, and Spectre v18.1. The
The iN5 standard-cell library contains 116 logic cells. 58 cells differ in logic function and/or drive strength; each of them has two versions of the Metal-1 wire locations (see Figures 4(b) and 4(c)). Typically, a library cell with base drive strength denoted by ‘X1’ or ‘D1’ in the cell name contains only the basic number of transistors that implements the cell’s logic function. We refer to these transistors as function transistors. Designers increase the drive strength for cells by adding so-called drive transistors in parallel with the function transistors. All these parallel transistors’ gates are controlled by the same input signal so that all these transistors can conduct or disconnect the same net pair at the same time, hence the drive strength is increased. In Figure 6, we show cell input count $n$, output count $m$, and the exhaustive fully-specified pattern count $m \times 2^n$ (every pattern contains a $n$-bit fully-specified stimulus pattern and a single-bit response).

4.1 Defect-Location Identification

For the 116 cells, we identified a total of 12,727 full-set open-defect locations; i.e. an average of 109.7 open-defect locations per cell, shown in Figure 7. However, to reduce the simulation time, we reduce the full set to a compact set based on fault equivalence. Only 47.9% representative opens are selected into the compact set that will be simulated. Many opens on the intra-cell interconnections are equivalent to transistor terminal opens. Therefore, only 1,531 out of 3,835 transistor-terminal opens non-equivalent to any interconnect opens are left.

An even larger reduction is obtained for the short-defect locations. The number of short locations in the compact set is reduced by 80.6% from the full set, shown in Figure 8. On average, 30.9 shorts are selected to the compact set per cell. Net-pair shorts in the compact set already cover 2,333 out of 2,616 transistor-terminal shorts, only 283 transistor-terminal shorts non-equivalent to the net-pair shorts need to be added to the compact set. For opens and shorts combined, the full set of defect locations over all iN5 library cells is reduced in the compact set by 73.8%, leading to a proportional reduction of analog simulation time in Step 2 of the CAT flow.

4.2 Defect Characterization

In this paper, we only consider “hard” open and short defects of which resistance values are 1000GΩ and 0Ω respectively in 108 combinational cells. The exhaustive set of fully-specified cell patterns are applied for each defect simulation iteratively. We call it one-cycle test pattern detection. Two-cycle cell pattern simulation uses from the exhaustive set of pattern pairs those pairs that cause a cell output to toggle. All these pattern pairs are concatenated into one waveform as the input signal of the simulation for each defect. With reusing the second pattern in each pattern pair as the first pattern of the next pattern pair, we reduce 50% pattern cycle count for the waveform. We run two-cycle pattern detection as top-off test of one-cycle detection to obtain higher fault coverage for cells. Even though two-cycle cell patterns help to detect more defects at cell level, there is a higher probability cell-to-chip expansion by ATPG fails than for one-cycle patterns. Therefore, one-cycle pattern detectable defects are preferred by ATPG.

Figure 9 shows the cumulative defect coverage of one-cycle and two-cycle patterns. The average defect coverage per cell is 71.5%. In cells with high drive strength, like BUFFD16, INVD8, and BUFFD8, low defect coverage is caused by many non-detectable open defects. These cells have many parallel drive transistors. For a group of parallel transistors controlled by the same input signal, an open defect on one transistor branch does not influence the other
branches, hence does not affect the cell’s logic function but drive strength. The two-cycle pattern detection is the most effective for the two most complex cells, full-adder cells, referring to Cell 105 and 106 in Figure 9. The simulation time for all 108 combinational cells was 6.3 hours.

The one-cycle and two-cycle detection results are encoded into a DDM for each cell. Figure 10 shows an example DDM in which defects are represented by columns and cell patterns by rows. If and only if cell pattern \( p \) detects defect \( d \), ‘1’ is marked in the matrix entry at the cross point of Column \( d \) and Row \( p \).

4.3 DDM Optimization

We extend each original DDM containing fully-specified patterns only with all partly-specified patterns that are implied by the original DDM [10]. Figure 11 shows the number of fully- and partly-specified patterns, and don’t-care bits in the extended DDM for each library cell. The first 27 cells on the horizontal axis are cells with one input, hence do not have any partly-specified patterns. For the other 87 cells, we identify 1204 partly-specified test patterns which contain a total of 1550 don’t-care bits. In Figure 12, we compared for each cell the average number of care bits per cell pattern for the original and extended DDMs. In library cells with more inputs more don’t care bits can be identified.

Based on the extended DDMs, we select a subset of DDM patterns with minimized care bit sum and full coverage of all detectable defects. This was proven to be an \( \mathcal{NP} \)-hard problem for which an innovative heuristic algorithm was proposed in [10]. For a total of 2,912 cell patterns in the extended DDMs for all cells in iN5, only 16.9% are selected as preferential patterns, and these preferential patterns contain only 13.4% of the total sum of care bits in all extended DDMs. The size of the pattern subset is a useful metric for how many patterns a particular library cell will need as a minimum.

5 IMEC iN5 vs. Cadence GPDK045

In this section, we compare the the standard cells of the iN5 node with a textbook-like, classical technology node. For this purpose, we chose Cadence’s GPDK045 45nm CMOS library [18] as a baseline. To enable a fair comparison, we select from both libraries 49 identified cells that have the same logic function and the same relative drive strength. The transistor numbers of iN5 cells are shown in Figure 13. The function transistor count increases with the number of cell inputs; they indicate the complexity of the cell design. The number of cell-internal nets always tracks the number of function transistors, as adding parallel drive transistors does not cause an increase in the number of nets. Compared with the 49 iN5 cells in Figure 13, all the GPDK045 counterparts, all types of cells are designed with the same number of function transistors, except cells XOR2X1 and XNOR2X1 that are implemented with two transistors more. Also, the number of drive transistors differs for only eight cells from these two libraries, despite the names of these cells indicate that they should have the same relative drive strength. In total, the 49 selected cells from the iN5 library have 26 transistors and 18 cell-internal nets more than their GPDK045 counterparts.

The comparison of the DLI results is shown in Table 1. Even though the iN5 cells’ structure is more complex than the GPDK045 cells’, the size of their full set of defect locations is smaller. This is because inside library cells, iN5 metal interconnections are in only one direction; the metal wires of the 45nm technology can flexibly change their directions between the \( x \) and \( y \) axes directions, so that a lot of 90\(^\circ\) bend corners exist in the GPDK045 cell layouts. Even though in iN5 cells, more interconnection layers and contacts be-

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**Table 1:** Comparison of defect-location numbers for GPDK045 and iN5.

<table>
<thead>
<tr>
<th></th>
<th>Full Set</th>
<th>Compact Set</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>#Opens</td>
<td>#Shorts</td>
</tr>
<tr>
<td>GPDK045</td>
<td>6,121</td>
<td>96,295</td>
</tr>
<tr>
<td>iN5</td>
<td>4,944</td>
<td>9,471</td>
</tr>
<tr>
<td>( \Delta )</td>
<td>-1,177</td>
<td>-86,824</td>
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tween the layers are designed to compensate some bend corners, most trivial bend corners are simplified into straight wires. The routing of each interconnection layer in iN5 actually is much simpler than in GPDK045. Bend corners are defect-sensitive points, hence 19.2% more open defect locations are identified based on these bend corners for the GPDK045 cells. Furthermore, the bend corners result in much more parasitic capacitors coupled between their locations and all the other different locations on each net, hence the GPDK045 cells have 90.2% more short locations in their full sets. However, the sizes of the compact sets are quite similar between the two libraries. In total, only two more defect locations are identified for the iN5 library, which causes the difference of defect characterization time to be negligible.

The defect coverage of most iN5 cells is higher than the GPDK045 cells, shown in Figure 14. On average, total defect coverages are 61.5% for the GPDK045 and 75.1% for the iN5 library.

For both libraries, the extended DDMs contain $2.5 \times \times$ the number of patterns in the original DDMs. The selected numbers of preferential patterns for both libraries are almost identical, which predicts ATPG will not need much more test patterns for circuits based on the iN5 library than when these circuits are based on GPDK045.

<table>
<thead>
<tr>
<th>#Original Patt.</th>
<th>#Extended Patt.</th>
<th>#Pref. Patt.</th>
<th>#Care Bits</th>
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<tbody>
<tr>
<td>GPDK045</td>
<td>406</td>
<td>1000</td>
<td>179 504</td>
</tr>
<tr>
<td>iN5</td>
<td>406</td>
<td>1000</td>
<td>181 512</td>
</tr>
<tr>
<td>Δ</td>
<td>0</td>
<td>0</td>
<td>+2 8</td>
</tr>
</tbody>
</table>

Table 2: Comparison of the number of patterns and care bits [10].

6 Conclusion

CAT improves test quality by explicitly targeting realistic cell-internal open and short defects by embedding dedicated cell-level test patterns in the overall chip-level test set. This paper is, to the best of our knowledge, the first to report on the application of CAT defect characterization on an advanced sub-10nm cell library.

In this paper, we used IMEC’s iN5 library, a standard-cell library in (what commercial founidries would refer to as) a 3nm CMOS technology. The technology uses advanced features, including FinFETs (with the number of fins per transistor reduced to one due to the small dimensions), an intermediate metal layer MINT, buried power rails, and metal wires per layer running in only one direction (i.e., either x or y axis direction).

We ran Cadence’s CAT library characterization tool flow on the iN5 library and compared the results of the various steps with results obtained on in logic function and drive-strength equivalent cells from the GPDK045 standard-cell library from Cadence [18] in a mature 45nm planar CMOS. Although the iN5 library-cell architecture comprises more layers than GPDK045 cells have, the number of identified non-equivalent potential open- and short-defect locations for both libraries is almost equal. Our DLI algorithms reduced the full set of defect locations with 73.5%, thereby reducing the defect simulation time for all 108 combinational library cells to 6.3 hours. The average defect coverage for hard open and short defects is 75.1%. Our DDM optimization algorithms found that to cover all detectable defects, we need on average 16.9% patterns as preferential cell patterns, and the preferential pattern set has only 13.4% care bits when compared to the exhaustive set of partially- and fully-specified cell patterns. Compared with the GPDK045 technology, the iN5 cells do not need more defect simulation time, but require slightly more care bits to cover more detectable defects. We intend to report on cell-aware ATPG results of circuits synthesized on the basis of the iN5 library in a future publication.

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