Course structure and organization

How will the course be presented?
Where can you find information?
How will you be graded?
Who, when, and how to contact?
Lecturers and TAs

Mitra Nasri
(course organizer and co-lecturer)

Twan Basten
(co-lecturer)

Marc Geilen
(co-lecturer)

Hossein Elahi
(main TA)

Joan Marce i Igual
(support TA)
Course knowledge goals

Module 1: Architecture
- System-on-chip architectures
  - Cache and memory organization;
  - On-chip networks (topologies, routing, deadlock analysis);

Module 2: OS support and programming models
- Operating system supports
  - Threads and processes;
  - Multiprocessor scheduling;
  - Communication and synchronization;
  - Data consistency;
- Programming models and paradigms
  - PThread, TBB, OpenMP, ...;

Module 3: Design-space exploration
- Mapping design space;
- Pareto analysis;
- Runtime adaptation and system scenarios;

Module 4: Models of computation
- Models of computation;
- Dataflow and design;

Weeks 1
- Hardware
- Operating system and software

Weeks 2
- Analysis techniques

Weeks 4, 5
- Modeling and analysis techniques

Weeks 6, 7
- Analysis techniques

Twan Basten
Mitra Nasri
Twan Basten
Marc Geilen
Course knowledge goals and you!

Module 1: Architecture
• System-on-chip architectures
  • Cache and memory organization;
  • On-chip networks (topologies, routing, deadlock analysis);

Module 2: OS support and programming models
• Operating system supports
  • Threads and processes;
  • Multiprocessor scheduling;
  • Communication and synchronization;
  • Data consistency;
• Programming models and paradigms
  • PThread, TBB, OpenMP, ...;

Module 3: Design-space exploration
• Mapping design space;
• Pareto analysis;
• Runtime adaptation and system scenarios;

Module 4: Models of computation
• Models of computation;
• Dataflow and design;

Knowledge needed to become a developer

Knowledge required to become a system architect

Architects
Developers
Testers
Course skill goals

- discrete-event modeling
- experimental research
- (peer) reviewing

You will learn them through the assignments

Logistics (related to Covid19)

- **No activity** (lecture, assignment, appointments, etc.) **on campus**
- The course is **fully online** (all activities including the exam are online)

- Most of the course follows a “blended education” style
  - You watch pre-recorded lectures
  - Then you attend the **live session**
  - **Live sessions** contain “exercises on the topic”, “Q&A”, or “more in-depth discussions”

- All live sessions will be **recorded**

- The communications happen on **MS Teams**

- Lecture materials, assignments, screencasts, or videos will be published on **CANVAS**
Organization

- 16 live lectures and (remote) labs
  - Monday, 8:45-10:30
  - Thursday, 13:30-15:15
  - (No classes during the Carnival break)
  - All lectures (first 6 weeks, 2017-2018 version) are available as a video lecture
- 3 practical assignments
- oral examination
Course and study material

- slides
- screencasts and videos of live sessions
- assignments
- POOSL
- background reading material
- multiprocessor basics test

all available through
- TU/e CANVAS, canvas.tue.nl

You must go through all activities of each Module on Canvas
You must watch all screencasts before attending the live session on that topic
How to join the course team on MS Teams

1. Open your MS Teams app (login with your TU/e credentials)

2. Go to “Teams”

3. Join team: EE_5LIE0 Multiprocessors - Q3 (2020-2021) using the option “Join a team with a code”

4. Enter the team’s code: n78umia
Channels:

- **A discussion channel for each assignment**
  - You can ask your questions about each assignment here from the TAs.
  - When needed, TA will create a private channel to discuss with you individually.
  - You can try to answer other student’s questions.
  - Active students on Teams who try to answer other’s questions will get “bonus points”.

- **A discussion channel for any question related to the lectures**

- **Link to the “Live sessions”**

- **Ticket for Assignment-Related Questions**
  - To get an appointment with the TA (mention the topic in your post)

- **Ticket for Content-Related Questions**
  - To get an appointment with a lecturer (mention the topic and the name of the lecturer in your post)

- **General**

- **Off topic**
  - For anything that is not “directly” related to the course, e.g., fun topics, anime, teaming up for extra activities, finding each other.
Getting a grade: assignments

All assignments are individual!

Typically C code

Parallel code

Implementation code

Assignment 1
interconnect analysis

HW/SW

Electronic Systems
Getting a grade: assignments

All assignments are individual!

Assignment 1
interconnect analysis

Assignment 2
design-space exploration

typically C code
parallel code
implementation code

HW/SW

<table>
<thead>
<tr>
<th>MIPS</th>
<th>MIPS</th>
<th>DSP</th>
<th>Acc</th>
<th>DSP</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Interconnect

DSP Memory Acc DSP

Electronic Systems
Getting a grade: assignments

All assignments are individual!

Assignment 1
interconnect analysis

Assignment 2
design-space exploration

Assignment 3
peer review

Assignments 1 & 2

typically C code

parallel code

implementation code

MIPS MIPS DSP Acc DSP
Interconnect

DSP Memory Acc DSP

HW/SW
Getting a grade: assignments

<table>
<thead>
<tr>
<th>Assignment</th>
<th>from</th>
<th>till</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assignment 1</td>
<td>4 February</td>
<td>5 March, 23:59h</td>
</tr>
<tr>
<td>interconnect analysis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assignment 2</td>
<td>25 February</td>
<td>26 March, 23:59h</td>
</tr>
<tr>
<td>design-space exploration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assignment 3</td>
<td>8 February</td>
<td>2 April, 23:59h</td>
</tr>
<tr>
<td>peer review</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Assignment schedule – for exact dates – check the assignment texts!

<table>
<thead>
<tr>
<th>weeks</th>
<th>wk 1</th>
<th>wk 2</th>
<th>wk 3</th>
<th>wk 4</th>
<th>wk 5</th>
<th>wk 6</th>
<th>wk 7</th>
<th>wk 8</th>
<th>wk 9</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Peer reviewing a1</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Peer reviewing a2</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Assignment 1: interconnect</td>
</tr>
</tbody>
</table>

Electronic Systems
## Getting a grade: assignments

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<tr>
<td>peer review</td>
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<td></td>
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</tbody>
</table>

**Deadlines are firm!**

- Deadline miss → Re-examination in Q4
- Re-examination failed → 2021
A note on **individual** assignments

- Discussions with fellow students are allowed, but
- All work (reports, models, scripts, programs, ...) **must be your own**.
- Your work will be **checked for plagiarism**!

- If copying of work is suspected, it will be taken to the examination committee.
  - In 2007, a student was suspended because of copying work.
  - In 2008, a student failed because of copying work.
  - In 2014, two students failed because of too close collaboration.

Start with the assignments as early as possible!

5 ECTS = 140 hours of study load

≈ 15 hours per week

≈ 2 full days (working 8 hours a day)
Getting a grade: oral exam

• Covers assignments and lectures.

• The (two) written and (two) received peer reviews are the basis.

• 45 mins + 15 mins evaluation

• You need to pass the multiprocessor basics test before registering

Check out the Study Guide for details!
Getting a grade: multiprocessor basics

• A CANVAS quiz

• published after completion of regular lectures in week 7

• that can be taken any time after publication, as often as you like

• and is passed with \( \geq 80\% \) correct answers

Check out the Study Guide for details!
Getting a grade: assignments + oral exam

<table>
<thead>
<tr>
<th>Assignment</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assignment 1: interconnect analysis</td>
<td>35%</td>
</tr>
<tr>
<td>Assignment 2: design-space exploration</td>
<td>40%</td>
</tr>
<tr>
<td>Assignment 3: peer review</td>
<td>25%</td>
</tr>
</tbody>
</table>

The oral exam determines the result!

Bonus for the oral exam:
Being active during the lectures and on Teams
Getting a grade: re-examination

- Q4, similar relative schedule

- Missing a deadline or failing the exam: retake the course in 2021
### Course schedule

#### Dates in 2021

#### Week 1

<table>
<thead>
<tr>
<th>wk</th>
<th>date</th>
<th>classes</th>
<th>assignments</th>
<th>study material</th>
<th>Lecturer</th>
</tr>
</thead>
</table>
| 1  | 1-2  | - course intro  
- course structure | - Slides and recorded video | Twan Basten and Mitra Nasri (live on MS Teams) |
|    |      | Live session | - Screencasts for [multiprocessor architecture, interconnect, and memory hierarchy](#) | Twan Basten (screencasts) |
|    |      | Live session during the timeslot of the course | - Screencasts for [experimental research](#) | Marc Geilen (screencasts) |
|    |      |      | - POOSL guide and screencasts;  
- Install POOSL. | TA (screencasts) |
| 4-2 |      | Introduction a1  
 a1 – interconnect analysis | - Assignment 1 text | Marc Geilen (live on MS Teams) |
|    |      | Live demo of POOSL | | TA (live on MS Teams) |
| 5-2 |      |      | - Screencasts for [OS support, data consistency, and synchronization](#) | Mitra Nasri (screencasts) |

Follow the schedule on CANVAS.
# Course schedule

## Week 1

<table>
<thead>
<tr>
<th>wk</th>
<th>date</th>
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<th>Lecturer</th>
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|    | 5-2  |         | - Screencasts for OS support, data consistency, and synchronization | Mitra Nasri (screencasts) | |

**Follow the schedule on CANVAS**

The person who oversees the item

**Things to do by yourself before the coming lecture**

You must watch the “screencasts” BEFORE the coming lecture
# Course schedule

## Follow the schedule on CANVAS

### Weeks 2, 3, 4, 5

<table>
<thead>
<tr>
<th>Date</th>
<th>Topic</th>
<th>Resources</th>
<th>Instructor</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-2</td>
<td>Q&amp;A session on architecture; OS support, data consistency, and synchronization; Introduction a3</td>
<td>- Recorded video - Slides and recorded video - Assignment 3 text</td>
<td>Twan Basten (live on MS Teams) Mitra Nasri (live on MS Teams)</td>
</tr>
<tr>
<td>9-2</td>
<td></td>
<td>- Screencasts for parallel programming models</td>
<td>Mitra Nasri (screencasts)</td>
</tr>
<tr>
<td>11-2</td>
<td>Parallel programming models</td>
<td>- Slides and recorded video</td>
<td>Mitra Nasri (live on MS Teams)</td>
</tr>
<tr>
<td>15-2</td>
<td>no classes – Carnival break</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18-2</td>
<td>no classes – Carnival break</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22-2</td>
<td>- Mapping design space; Mapping tasks to processors; Pareto analysis</td>
<td>- Slides and recorded video</td>
<td>Twan Basten (live on MS Teams)</td>
</tr>
<tr>
<td>25-2</td>
<td>Introduction a2</td>
<td>- Assignment 2 text</td>
<td>Marc Geilen (live on MS Teams)</td>
</tr>
<tr>
<td></td>
<td>lab (contact TA)</td>
<td></td>
<td>TA (by appointment)</td>
</tr>
<tr>
<td>1-3</td>
<td>- Run-time adaptation; System scenarios</td>
<td>- Slides and recorded video</td>
<td>Twan Basten (live on MS Teams)</td>
</tr>
<tr>
<td>4-3</td>
<td>lab (contact TA)</td>
<td></td>
<td>TA (by appointment)</td>
</tr>
<tr>
<td>5-3</td>
<td></td>
<td></td>
<td>deadline: a1</td>
</tr>
</tbody>
</table>
CANVAS

canvas.tue.nl – 5LIE0 – multiprocessors

and the

Study Guide
Contact emails

- Mitra Nasri (course organizer and co-lecturer)
  m.nasri@tue.nl

- Twan Basten (co-lecturer)
  a.a.basten@tue.nl

- Marc Geilen (co-lecturer)
  m.c.w.geilen@tue.nl

- Hossein Elahi (main teaching assistant (TA))
  g.elahi@tue.nl

- Joan Marce i Igual (support teaching assistant (TA))
  j.marce.i.igual@tue.nl