EINDHOVEN UNIVERSITY OF TECHNOLOGY

Multiprocessors

(5LIE0)

Lecture 1

Lecturers

Mitra Nasri, Twan Basten, Marc Geilen

Teaching Assistants (TAs)

Joan Marce i Igual (main TA), Hossein Elahi (support TA)

Department of Electrical Engineering

Electronic Systems

Course structure and organization

How will the course be presented?

Where can you find information?

How will you be graded?

Who, when, and how to contact?

Lecturers and TAs

Mitra Nasri
(course organizer and co-lecturer)

Twan Basten
(co-lecturer)

Marc Geilen
(co-lecturer)

Joan Marce i Igual
(main TA)

Hossein Elahi
(support TA)

Course knowledge goals

Module 1: Architecture

Hardware — **Week 1** — **Twan Basten**

- System-on-chip architectures
  - Cache and memory organization;
  - On-chip networks (topologies, routing, deadlock analysis);

Module 2: OS support and programming models

Operating system and software — **Week 2** — **Mitra Nasri**

- Operating system supports
  - Threads and processes;
  - Multiprocessor scheduling;
  - Communication and synchronization;
  - Data consistency;
- Programming models and paradigms
  - PThread, TBB, OpenMP, …;

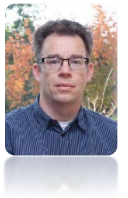
Module 3: Design-space exploration

Analysis techniques — **Weeks 3, 4** — **Twan Basten**

- Mapping design space;
- Pareto analysis;
- Runtime adaptation and system scenarios;

Module 4: Models of computation

Modeling and analysis techniques — **Weeks 5, 6** — **Marc Geilen**



- Models of computation;
- Dataflow and design;

Course knowledge goals and you!

Module 1: Architecture

Hardware

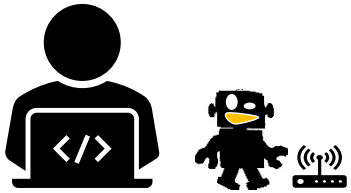
- System-on-chip architectures
  - Cache and memory organization;
  - On-chip networks (topologies, routing, deadlock analysis);

Module 2: OS support and programming models

Operating system and software

- Operating system supports
  - Threads and processes;
  - Multiprocessor scheduling;
  - Communication and synchronization;
  - Data consistency;
- Programming models and paradigms
  - PThread, TBB, OpenMP, …;

Knowledge needed to become a developer



Module 3: Design-space exploration

Analysis techniques

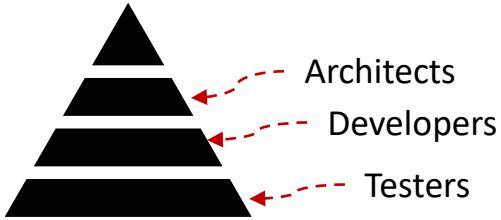
- Mapping design space;
- Pareto analysis;
- Runtime adaptation and system scenarios;

Module 4: Models of computation

Modeling techniques

- Models of computation;
- Dataflow and design;

Knowledge required to become a system architect



Course skill goals

- discrete-event modeling
- experimental research
- (peer) reviewing

You will learn them through the assignments

Image source: https://social.usq.edu.au/study-tips/blogs/how-to-get-assignment-started-kristen

Logistics (related to Covid19)

- **Lectures and lab hours will be on campus**

- The course follows a “blended education” style
  - You watch short pre-recorded lectures
  - Then you attend the **lecture**
  - **Lectures** contain “exercises on the topic”, “Q&A”, or “more in-depth discussions”

- The lectures will not be recorded (however, we will make the recording of the lectures of last year available to you)

- The communications happen on **MS Teams** (you will be automatically invited to the team of the course): **5LIE0 (2021-GS3) Multiprocessors**

- Lecture materials, assignments, screencasts, or videos will be published on **CANVAS**

Organization

- About 16 live lectures and lab sessions
  - Monday, 8:45-10:30
  - Thursday, 13:30-15:15
  - (No classes or lab sessions during the Carnival break)
  - A recorded version of the lectures (from 2021) are available on Canvas
- 3 practical assignments
- oral examination

Course and study material

- slides
- screencasts and videos
- assignments
- POOSL
- background reading material
- multiprocessor basics test

all available through

- TU/e CANVAS, canvas.tue.nl

- You **must** go through all activities of each **Module** on **Canvas**
- You **must** watch all screencasts before attending the live session on that topic

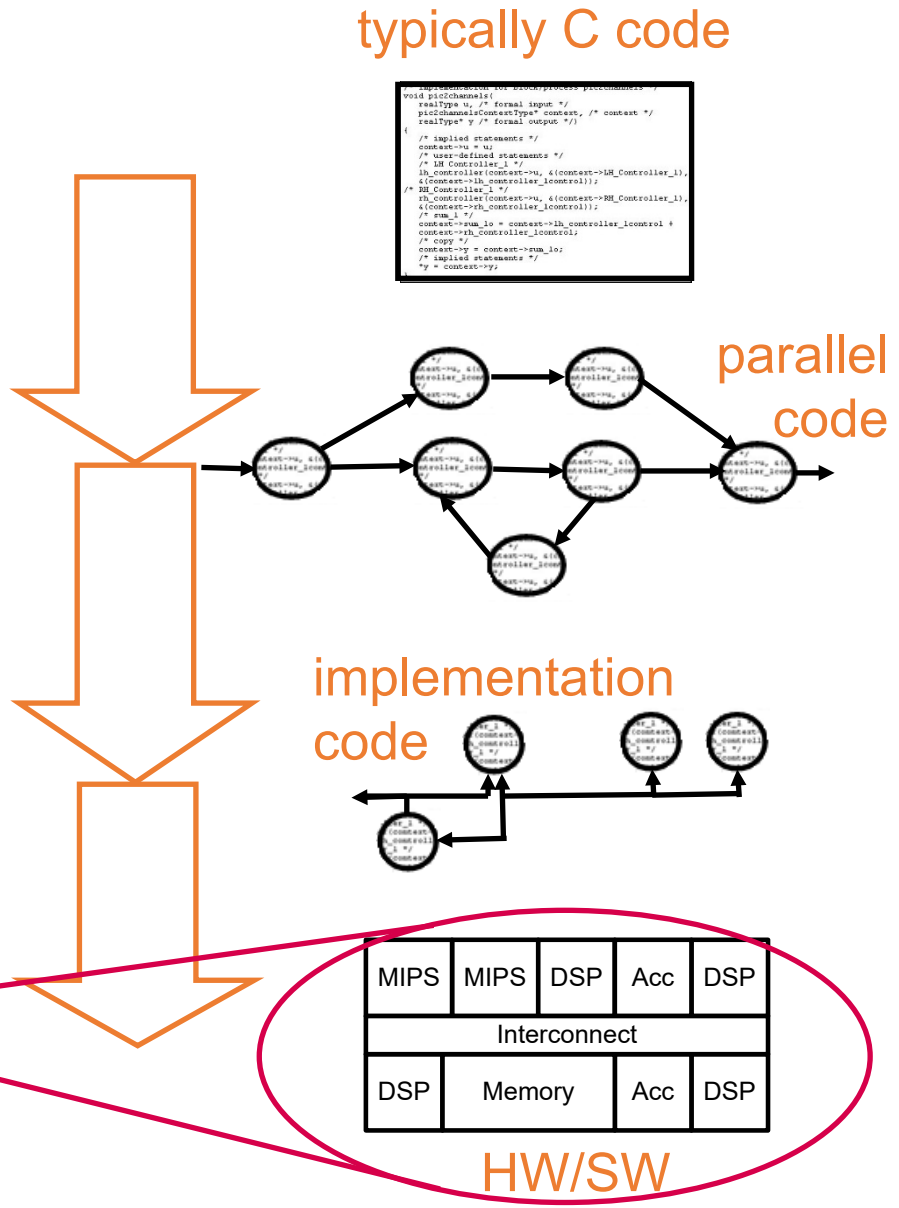
Course's Team EE_5LIE0 (2021-2022)

- Channels:
  - **A discussion channel for each assignment**
    - Ask your questions about the assignments during the lab hours.
    - You can also ask your generic questions about each assignment on this channel.
    - When needed, **TAs** will create a private channel to discuss with you individually.
    - You can try to answer other student's questions.
    - Active students on Teams who try to answer other's questions will get "**bonus points**".
  - **A discussion channel for any question related to the lectures**
  - **General**
  - **Off topic**
    - For anything that is not "directly" related to the course, e.g., fun topics, anime, teaming up for extra activities, finding each other.

Getting a grade: assignments

All assignments are individual!

Estimated workload:
40 hours



Assignment 1
interconnect analysis

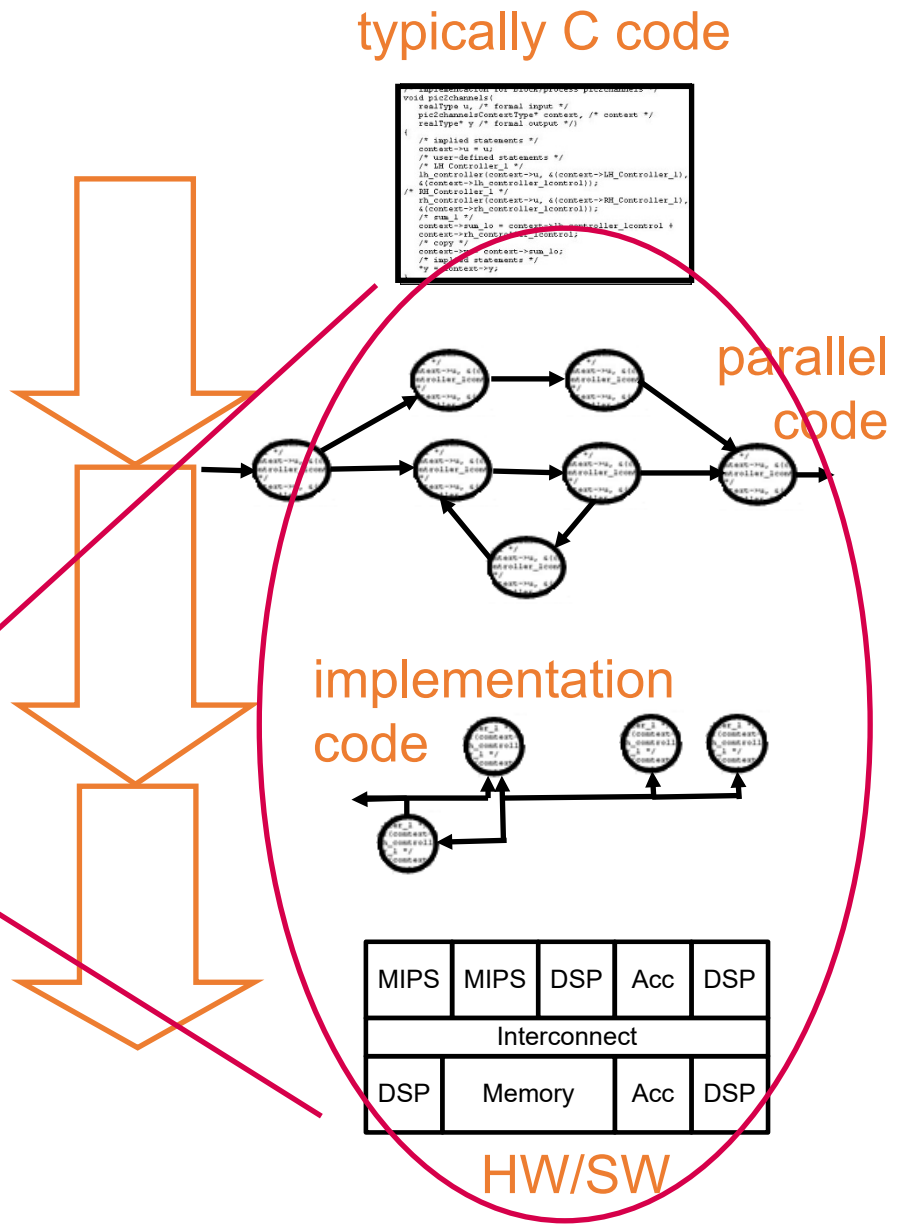
Getting a grade: assignments

All assignments are individual!

Estimated workload:
40 hours

Assignment 2
design-space exploration

Assignment 1
interconnect analysis



Getting a grade: assignments

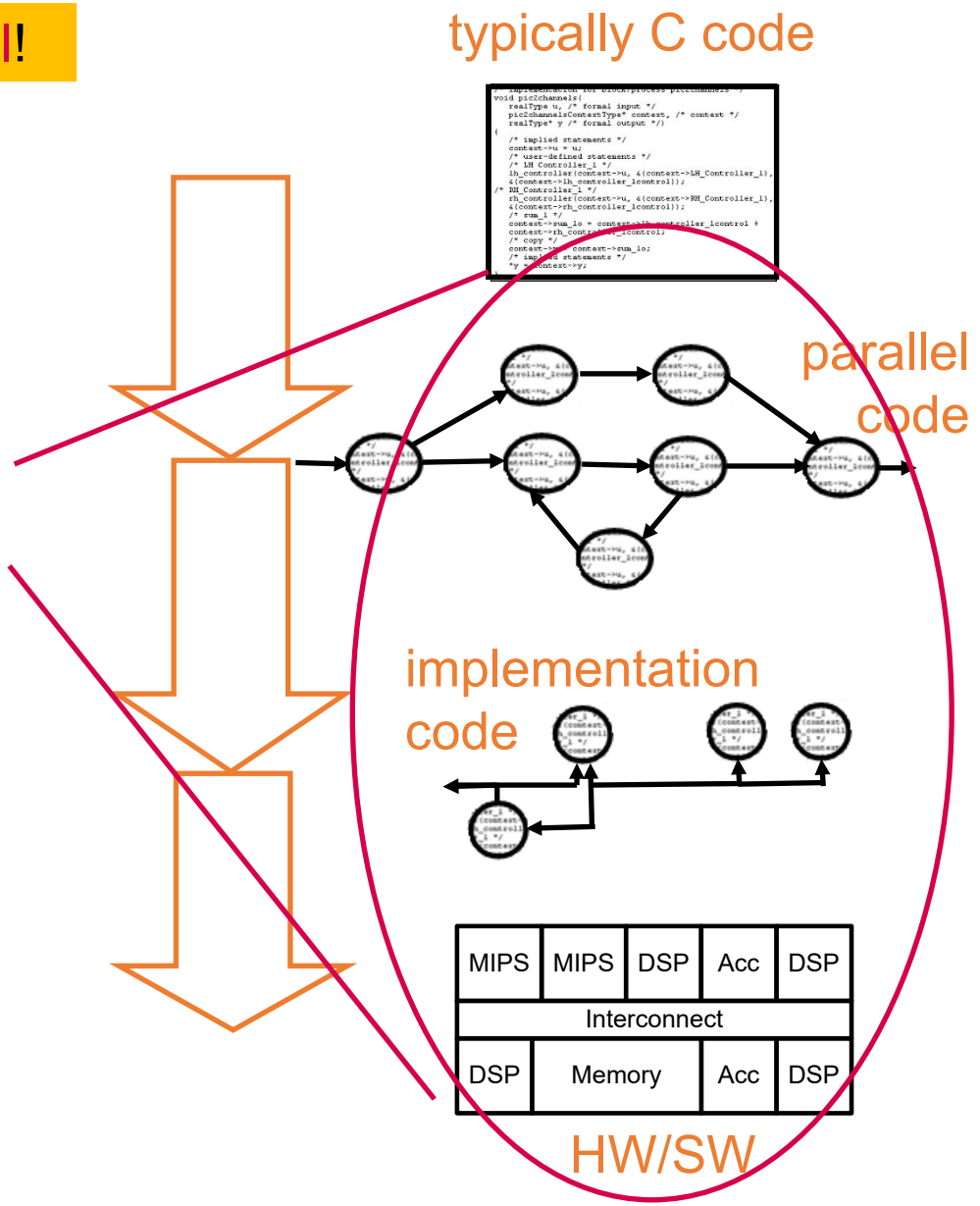
All assignments are individual!

Estimated workload:
16 hours

Assignment 3
peer review
Assignments 1 & 2

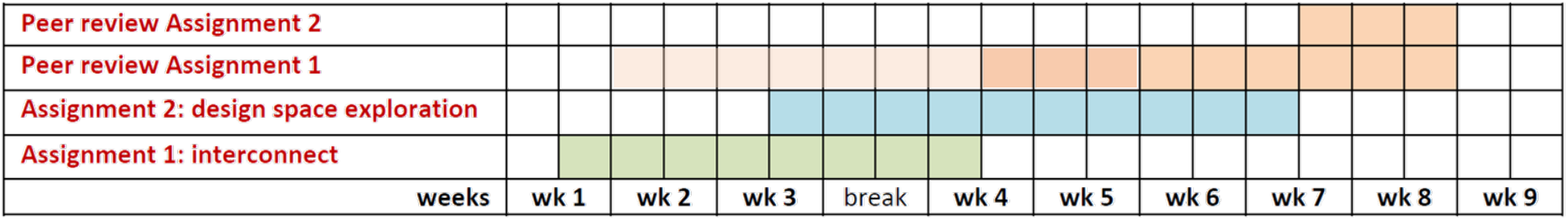
Assignment 2
design-space exploration

Assignment 1
interconnect analysis



Getting a grade: assignments

	from	till
Assignment 1 interconnect analysis	10 February	9 March, 23:59h
Assignment 2 design-space exploration	24 February	30 March, 23:59h
Assignment 3 peer review	Introduced on 14 February Started from 10 March	8 April, 23:59h



A1: 40h, A2: 40h, A3:16h, lectures: 44

Getting a grade: assignments

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Deadlines are firm!

Deadline miss → Re-examination in Q4

Re-examination failed → re-take the course next year

A note on individual assignments

- Discussions with fellow students are allowed, but
- All work (reports, models, scripts, programs, …) must be your own.
- Your work will be checked for plagiarism!

- If copying of work is suspected, it will be taken to the examination committee.
  - In 2007, a student was suspended because of copying work.
  - In 2008, a student failed because of copying work.
  - In 2014, two students failed because of too close collaboration.

Start with the assignments as early as possible!

5 ECTS = 140 hours of study load

≈ 15 hours per week

≈ 2 full days (working 8 hours a day)

Getting a grade: oral exam

- Covers assignments and lectures.
- The (two) written and (two) received peer reviews are the basis.
- 45 mins + 15 mins evaluation
- You need to pass the multiprocessor basics test before registering

Check out the **Study Guide** for details !

Getting a grade: multiprocessor basics

- A CANVAS quiz
- published after completion of regular lectures in week 7
- that can be taken any time after publication, as often as you like
- and is passed with >= 80% correct answers

Check out the **Study Guide** for details !

Getting a grade: assignments + oral exam

	weight
Assignment 1 interconnect analysis	**35%**
Assignment 2 design-space exploration	**40%**
Assignment 3 peer review	**25%**

The **oral exam** determines the result!

Bonus for the oral exam:
Being active during the **lectures and on Teams**

Getting a grade: re-examination

- Q4, similar relative schedule

- Missing a deadline or failing the exam: retake the course next academic year

Course schedule

Dates

The person who oversees the item

Week 1

wk	date	classes	assignments	study material	Lecturer
1	7-2	**- course intro** **- course structure** (topic)		- Slides (Location of the activity)	**Twan Basten** and **Mitra Nasri** (on campus)
		Lecture (during the course timeslot)		- Screencasts for **multiprocessor architecture, interconnect, and memory hierarchy**	**Twan Basten** (screencasts)
				- Screencasts for **experimental research**	**Marc Geilen** (screencasts)
		Lab (during the course timeslot)		- POOSL guide and screencasts; - Install POOSL.	**TA** (screencasts)
	10-2	**Introduction a1**	**a1 – interconnect analysis**	**- Assignment 1 text**	**Marc Geilen** (on campus)
		Live demo of POOSL			**TA** (on campus)
	10-2			- Screencasts for **OS support, data consistency, and synchronization**	**Mitra Nasri** (screencasts)

Week number

Follow the schedule on **CANVAS**

Course schedule

The person who oversees the item

wk	date	classes	assignments	study material	Lecturer
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	10-2	**Introduction a1** **Live demo of POOSL**	**a1 – interconnect analysis**	**- Assignment 1 text**	**Marc Geilen** (on campus) **TA** (on campus)
	10-2			- Screencasts for **OS support, data consistency, and synchronization**	**Mitra Nasri** (screencasts)

Current lecture

Coming session

Things to do by yourself before the coming lecture

You must watch the “screencasts” BEFORE the coming lecture

Course info

CANVAS

canvas.tue.nl – 5LIE0 – multiprocessors

and the
Study Guide

Contact emails

- Mitra Nasri (course organizer and co-lecturer)
  m.nasri@tue.nl

- Twan Basten (co-lecturer)
  a.a.basten@tue.nl

- Marc Geilen (co-lecturer)
  m.c.w.geilen@tue.nl

- Joan Marce i Igual (main teaching assistant (TA))
  j.marce.i.igual@tue.nl

- Hossein Elahi (support teaching assistant (TA))
  g.elahi@tue.nl