

## **A) Branch Prediction**

# branch predictor type {nottaken|taken|perfect|bimod|2lev|comb}

-bpred                      bimod

# bimodal predictor config (<table size>)

-bpred:bimod                2048

# 2-level predictor config (<l1size> <l2size> <hist\_size> <xor>)

-bpred:2lev                 1 1024 8 0

# combining predictor config (<meta\_table\_size>)

-bpred:comb                 1024

# return address stack size (0 for no return stack)

-bpred:ras                  8

# BTB config (<num\_sets> <associativity>)

-bpred:btb                  512 4

*Note: Besides the textbook and slides, please also refer to:*

1) *wiki ([http://en.wikipedia.org/wiki/Branch\\_predictor](http://en.wikipedia.org/wiki/Branch_predictor))*

2) *Yale N. Patt's papers like "A comparison of dynamic branch predictors that use two levels of branch history", "Using Hybrid Branch Predictors to Improve Branch Prediction in the Presence of Context Switches"*

## **B) Memory System**

# l1 data cache config, i.e., {<config>|none}

-cache:dl1                  dl1:128:32:4:1

# l2 data cache config, i.e., {<config>|none}

-cache:dl2                  ul2:1024:64:4:1

# l1 inst cache config, i.e., {<config>|dl1|dl2|none}

-cache:il1                  il1:512:32:1:1

# l2 instruction cache config, i.e., {<config>|dl2|none}

-cache:il2                  dl2

# instruction TLB config, i.e., {<config>|none}

-tlb:itlb                    itlb:16:4096:4:1

# data TLB config, i.e., {<config>|none}

-tlb:dtlb                    dtlb:32:4096:4:1

### C) Function Units

# total number of integer ALUs available

-res:ialu 4

# total number of integer multiplier/dividers available

-res:imult 1

# total number of floating point ALUs available

-res:fpalu 4

# total number of floating point multiplier/dividers available

-res:fpmult 1

### D) Data Path & Others

# instruction fetch queue size (in insts)

-fetch:ifqsize 4

# instruction decode B/W (insts/cycle)

-decode:width 4

# instruction issue B/W (insts/cycle)

-issue:width 4

# run pipeline with in-order issue

-issue:inorder false

# issue instructions down wrong execution paths

-issue:wrongpath true

# instruction commit B/W (insts/cycle)

-commit:width 4

# register update unit (RUU) size

-ruu:size 16

# load/store queue (LSQ) size

-lsq:size 8

**Note: These are the parameters (with their default values) you can tune. Please keep the values of **other** parameters **unchanged** unless you have good reasons (explain it in your report)!**